INDUCTIVE LOAD TESTER

MODEL 9302-LV/9303-PU/9304-HB

INSTRUCTION MANUAL

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APPENDIX

TESEC

INDUCTIVE LOAD TESTER

MODEL 9302-LV/9303-PU/9304-HB

INSTRUCTION MANUAL
FOR
HARDWARE

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GENERAL DESCRIPTION

With the increasing demands for quality, we introduce the Inductive Load Tester 9302-LV/9303-PU, a new test system specifically designed for inductive-breakdown evaluation.

Since transistors and MOSFETs are used in switching power supplies, auto motive ignitions and relay-drive circuits are subject to a substantial voltage surge across the inductor when the current is turned off, it is very essential to accurately reproduce this surge when the device is being tested.

Model 9302-LV/9303-PU accomplishes the following features through the use of inductor modules that plug into the tester. The tester is then programmed for collector current, base current, high and low current limits, gate voltage, etc. Each device is tested for its sustaining voltage and its reverse-bias safe operating area is defined.
For high volume environments, it can be interfaced to all the TESEC discrete handlers to provide large output.

Features

(1) Measurement can be performed at any V_{CEO}, V_{CEX}, and V_{CER} condition.
(2) Constant-current mode or constant-voltage mode of collector power supply can be selected.
(3) Clamp measurement or non-clamp mesurement can be selected.
(4) NPN and PNP measurements can be performed with one set of test head.
(5) Multi-testing can be performed. Up to 3 tests can be performed under the different conditions.
(6) Repeat test can be performed up to 250 times.
(7) Sixteen test programs can be memorized in the tester. (A backup battery is used.)
(8) An LCD of 42 columns and 16 rows is used as the display.
(9) A comment can be indicated on the display.
(10) A buzzer is activated for a programmed period of time at the occurrence of FAIL.
(11) The tester can be controlled externally through the GP-IB or RS-232-C interface.
(12) The tester can be interfaced to a handler by means of a test head.

1. SPECIFICATIONS

1.1 Measurement Range

(1) Polarity : NPN/PNP, N-FET/P-FET

(2) Measurement range : 30 ~ 2000 V (Accuracy ±2%)

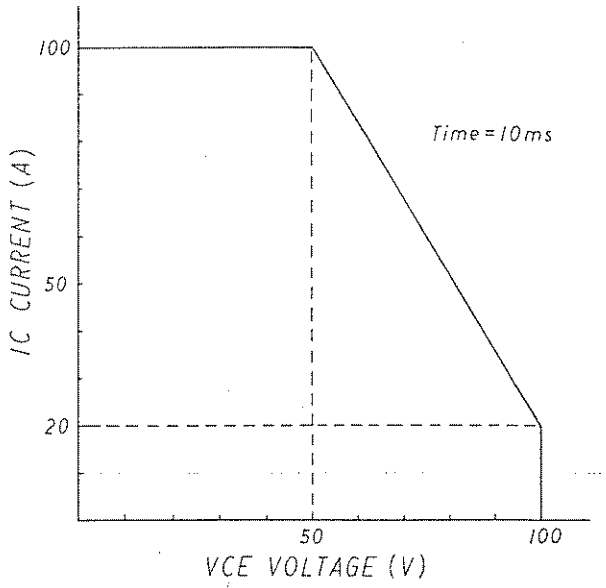
1.2 Range of Settings

Item	Range	Step	Accuracy
Collector current I_C/I_D	1.0 ~ 100.0 A	0.1 A	±(2% + 0.4 A)
Collector voltage V_C/V_D *1	1.0 ~ 100.0 V	0.1 V	±2%
Base current I_B	0.01 ~ 20.00 A	0.01 A	±10%
Reverse-bias base current I_{BR} *2	0.01 ~ 20.00 A	0.01 A	±10%
Gate voltage V_G	1.0 ~ 30.0 V	0.1 V	±(2%+0.6V)
Reverse-bias gate voltage V_{GR} *2	1.0 ~ 30.0 V	0.1 V	±(2%+0.6V)
Clamp voltage V-CLAMP	VC=OFF 40~2000 V	1 V	±1%
	VC=ON 30~2000 V		
Voltage limit V-GATE	30 ~ 2000 V	1 V	±(2%+8V)
IH limit I_H	0.1 ~ 100.0 A	0.1 A	±(2%+0.4A)
IL limit I_L	0.1 ~ 100.0 A	0.1 A	±(2%+0.4A)

Notes: *1 Valid when VC ON is set at the front panel (constant-voltage system).

*2 Valid when REVERSE ON is set at the front panel.

1.3 Forcing Power Range Diagram



1.4 Inductance (optional)

50 μH, 100 μH, 200 μH, 300 μH, 500 μH (at 2000 V, 100 A), 1 mH (at 2000 V, 50 A)

1.5 Functions

VC ON	Enables the collector power supply to be in constant-voltage mode. Set the collector voltage V_C and collector current I_C.
VC OFF	Enables the collector power supply to be in constant-current mode. Set the collector current I_C. The maximum collector voltage is about 40 volts.
REVERSE ON	Enables to measure V_{CEX}. Set the reverse-bias base current I_{BR} or reverse-bias gate voltage V_{GR}.
REVERSE OFF	Enables to measure V_{CEO} and V_{CER}. The terminal B(G) is measured without bias when I_B is turned off.
V-CLAMP ON	Enables to do clamp-measurement. Set the clamp-voltage V-CLAMP.
V-CLAMP OFF	Enables to do non-clamp measurement.
REPEAT	Enables to do maximum 250 continuous measurements under the same condition.
MULTI TEST	Enables to do maximum 3 continuous measurements under the different conditions.
SINGLE TEST	Enables to do normal test one by one.

1.6 Programming

(1) By the key switches on the front panel

(2) By an external CPU through the GP-IB or RS-232-C interface

16 test programs can be memorized in the tester which is provided with the backup battery.

1.7 Test Result Display

(1) VCE(SUS) OOOO V

When REVERSE OFF is set, the $V_{(SUS)}$ value specified by the I_H is displayed.

(2) VCEX(SUS) OOOO V

When REVERSE ON is set to, the $V_{(SUS)}$ value specified by the I_H is displayed.

(3) PASS, FAIL1, FAIL2, PRE-OPEN, PRE-SHORT, POST-OPEN, POST-SHORT, IC-ERROR

PASS	$V_{CE} \geq$ V-GATE at the range between I_H and I_L
FAIL1	$V_{CE} <$ V-GATE at the range between I_H and I_L
FAIL2	$V_{CE} <$ V-GATE at I_H
PRE-OPEN	Even if I_B power booster is on before VSUS test, the I_C current is one-fifth of the specified current or less.
PRE-SHORT	Even if I_B power booster is off before VSUS test, the I_C current is one-fifth of the specified current or more.
POST-OPEN	At repeat test or multi-test, even if I_B power booster is on after the 1st VSUS test, the I_C current is one fifth of the specified current or less.
POST-SHORT	Even if I_B booster is off after VSUS test, the I_C current is one-fifth of the specified current or more.
IC-ERROR	The I_C current does not reach the specified current.

(4) Display Unit LCD for 42 columns and 16 rows with a backlight

(5) Binning

4-bin mode is displayed at the front panel of a test head.

PASS

FAIL1

FAIL2

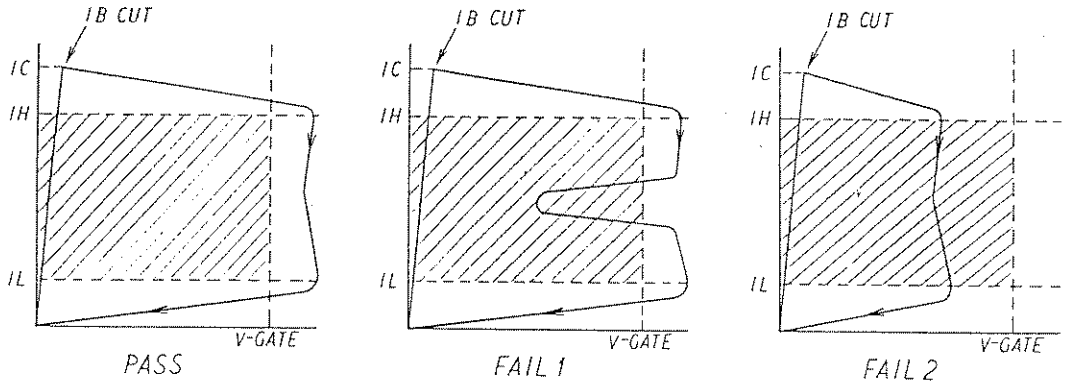
REJECT..... PRE-OPEN
PRE-SHORT
POST-OPEN
POST-SHORT
IC-ERROR

(6) SOA Evaluation

PASS — A device passes the reverse-bias SOA test if V_{CE} remains outside the shaded area shown in the figure below. V_{CE} is measured at I_H and displayed as $V_{CE(SUS)}$.

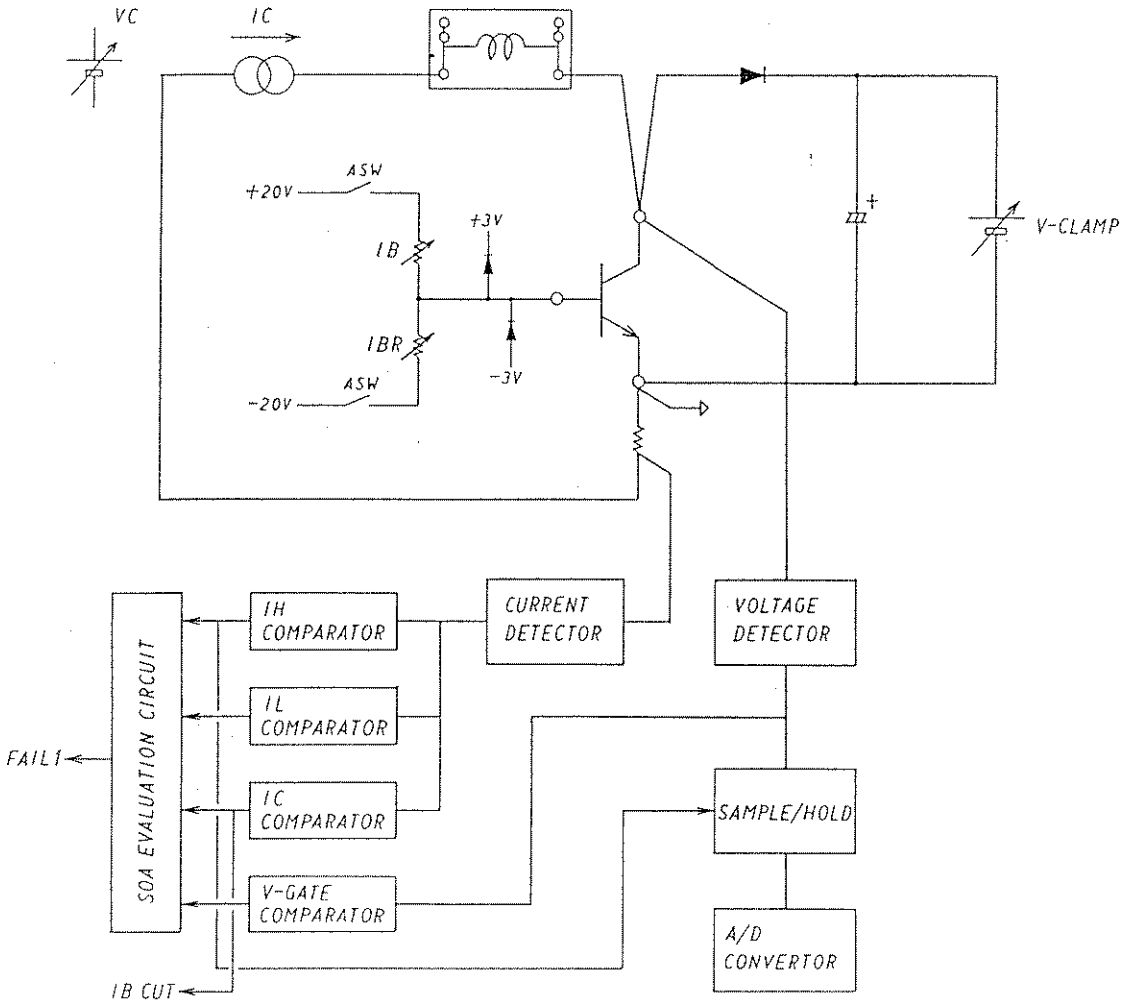
FAIL1 — A device fails the reverse-bias SOA test if V_{CE} enters the shaded area as shown below.

FAIL2 — A device fails the reverse-bias SOA test if V_{CE} does not reach V-GATE.

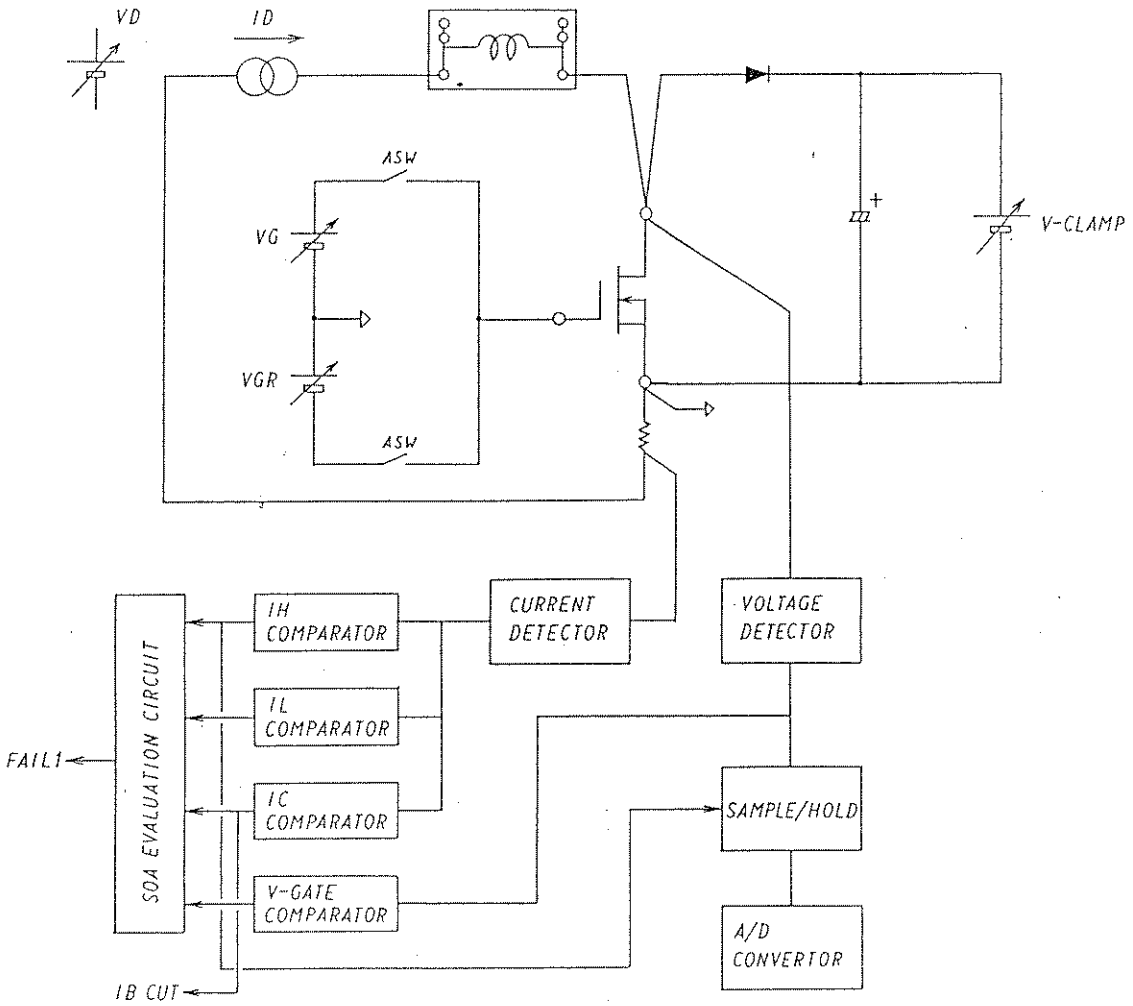


1.8 Fundamental Measurement Circuits

(1) NPN

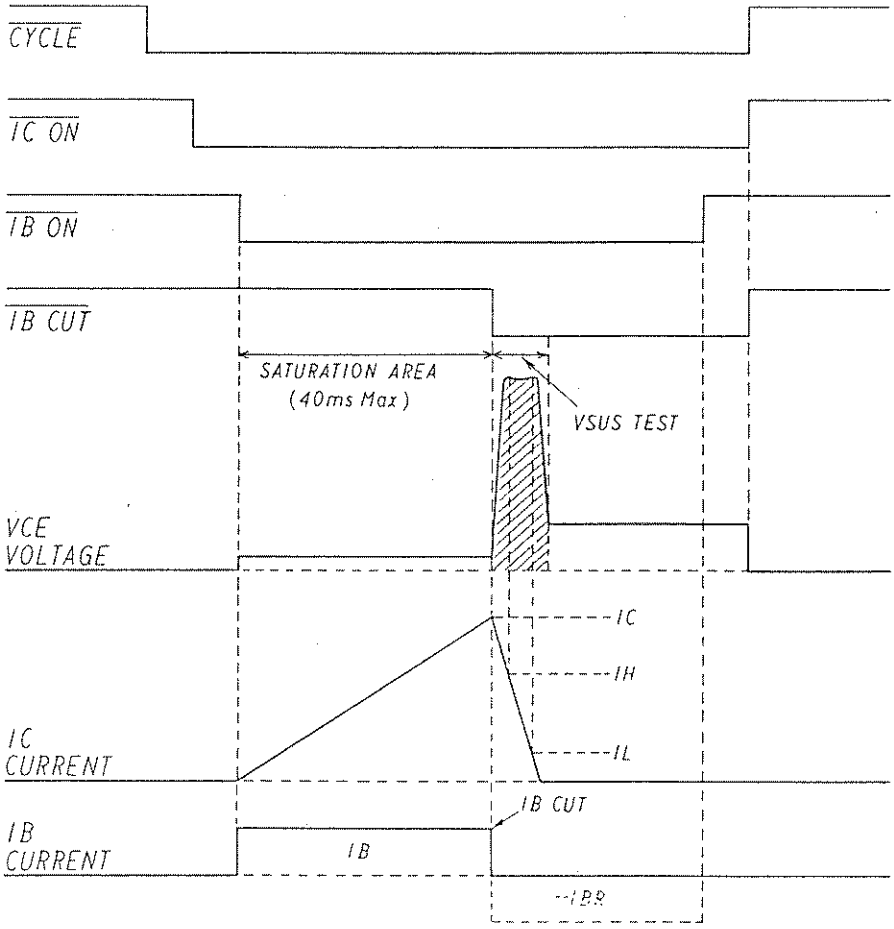


(2) N-FET

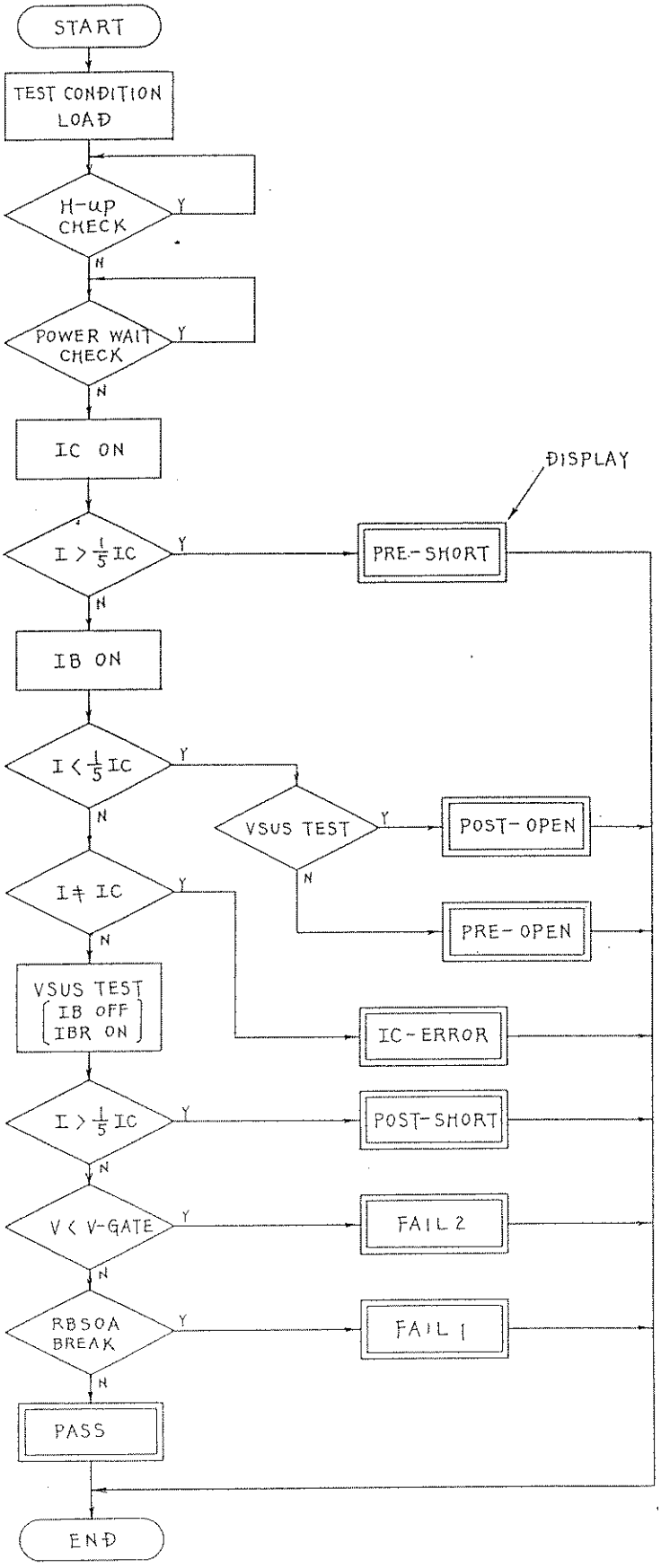

VD
ID
ASW
VG
VGR
ASW
V-CLAMP
IH COMPARATOR
IL COMPARATOR
IC COMPARATOR
V-GATE COMPARATOR
SOA EVALUATION CIRCUIT
FAIL1
IB CUT
CURRENT DETECTOR
VOLTAGE DETECTOR
SAMPLE/HOLD
A/D CONVERTOR

1.9 Timing Chart

The relation between the logic signal waveforms at the check terminals of the 9302-LV rear panel and the voltage and current waveforms of DUT are shown below.



1.10 Flowchart



1.11 Interface Specifications

1.11.1 GP-IB Connectors

(1) Pin arrangement

GP-IB ADS-B24FDE(HONDA)Male			
Pin No.	Signal	Pin No.	Signal
1	DI01	13	DI05
2	DI02	14	DI06
3	DI03	15	DI07
4	DI04	16	DI08
5	EOI	17	REN
6	DAV	18	GND
7	NRFD	19	GND
8	NDAC	20	GND
9	IFC	21	GND
10	SRQ	22	GND
11	ATN	23	GND
12	SHIELD	24	LOGIC GND

(2) Connectors

(a) 9302-LV side : ADS-B24FDE (HONDA)

(b) Cable side : 408JE (DDK) or equivalent

(3) DIP switch setting

The relationship between the stations and addresses, and the setting of the bit switches of the DIP switch SW2 in the rear panel are as follows:

Station	Address	SW2 No.				
		1	2	3	4	5
A-station	11	1	1	0	1	0
B-station	12	0	0	1	1	0
C-station	13	1	0	1	1	0
D-station	14	0	1	1	1	0
F-station	15	1	1	1	1	0

1.11.2 HANDLER Connectors

(1) Pin arrangement

HANDLER 57GE-40140-751 (DDK)			
Pin No.	Signal	Pin No.	Signal
1	PASS-L	7	END-L
2	LOW-L	8	–
3	HIGH-L / FAIL-L	9	GND
4	REJECT-L	10	SHIELD
5	RETURN (+12 V)	11	–
6	START-L	12	+12 V - KT
		13*1	–
		14*1	–

Note : "-L" indicates a low true.

(2) Connectors

	S/No. 0008 or before	S/No. 0009 or later
(a) 9302-LV side	SD-1612A (HRS)	57GE-40140-751 (DDK)
(b) Cable side	P-1612BA-C (HRS) *1: Asterisked pins are not provided.	57-30140 (DDK)

(3) Test start (START) signal

- Low true is set at the time of shipment. (Switching to high true can be made by the DIP switch SW4-3 to SW4-6.)
- Required signal pulse : 1 ms

(4) Test end (End) signal

- Low true is set at the time of shipment. (Switching to high true can be made by the DIP switch SW4-2.)
- Required signal pulse : 3 ms

(5) Bin signals

- Low true is set at the time of shipment. (Switching to high true can be made by the DIP switch SW4-1.)
- Output signal : Hold

(a) 2-bin mode

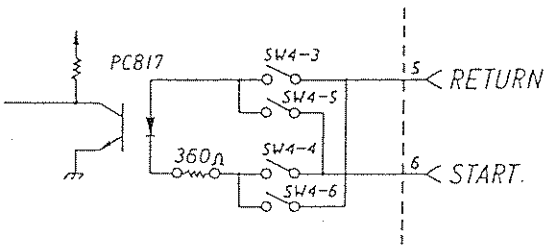
PASS, FAIL (FAIL1, FAIL2, REJECT)

(b) 4-bin mode

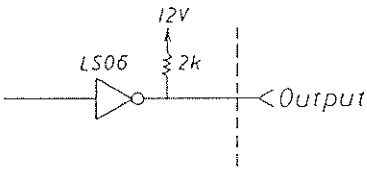
PASS, FAIL1, FAIL2, REJECT (PRE-OPEN, PRE-SHORT, POST-OPEN, POST-SHORT, IC-ERROR)

(6) Interface circuits

(a) Input circuit (START signal)



(b) Output circuits (END, bin signals)



(7) DIP switch setting

Logic setting (high true and low true) is made by the DIP switch SW4 on the rear panel of the 9302-LV.

SW4		
SW No.	ON	OFF
1	SORT-H	SORT-L
2	END-H	END-L
3	START-L	
4	(No. 5, 6 = OFF)	
5	START-H	
6	(No. 3, 4 = OFF)	
7	–	–

Note :

(a) SORT = PASS, FAIL
PASS, FAIL1, FAIL2, REJECT

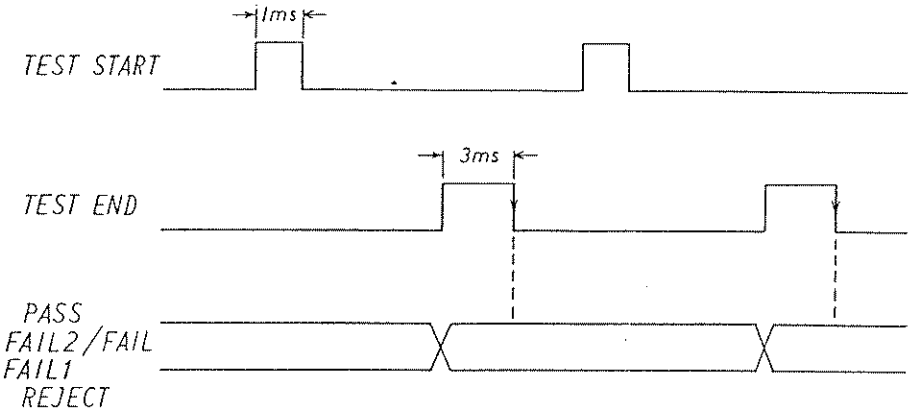
(b) When the switches, No.3 and No.4 are turned ON, the switches No.5 and No.6 must be turned OFF.

(c) When the switches, No.5 and No.6 are turned ON, the switches No.3 and No.4 must be turned OFF.

(d) The SW4 switch is set to conform to the interface specifications at the time of shipment.

(e) "-H" indicates high true and "-L" indicates low true.

(8) Timing chart



Note : A bin signal is output at the start of a leading edge of an END signal and is held till the test result changes. At the start of trailing edge of the END signal, the interfaced apparatus triggers to latch the bin signal.

1.11.3 PARALLEL Connector (Centronics interface)

(1) Pin arrangement

PARALLEL DB-25ST-N-S1 (JAE) Female			
Pin No.	Signal	Pin No.	Signal
1	DSTB-L	14	–
2	DATA0-H	15	(FAULT)
3	DATA1-H	16	(PRIME)
4	DATA2-H	17	–
5	DATA3-H	18	GND
6	DATA4-H	19	GND
7	DATA5-H	20	GND
8	DATA6-H	21	GND
9	DATA7-H	22	GND
10	ACK-L	23	GND
11	BUSY-H	24	GND
12	–	25	GND
13	–		

Notes:

(a) Each signal in parenthesis ( ) is set to be open on the PT9129 connector board.

(b) "-H" indicates high true and "-L" indicates low true.

(2) Connectors

(a) 9302-LV side : DB-25ST-N-S1 (JAE)
Tow lock screws (#4-40) are used.

(b) Cable side : DB-25P-N (JAE) or equivalent

1.11.4 EXT Connector

(1) Pin arrangement

EXT 57GE-40240-751 (DDK) Male			
Pin No.	Signal	Pin No.	Signal
1	AUXX-L	13	AUXY-L
2	AUXZ-L	14	(N-H / P-L)*1
3	+5V-T	15	WAIT-L
4	800-L	16	400-L
5	200-L	17	100-L
6	80-L	18	40-L
7	20-L	19	10-L
8	8-L	20	4-L
9	2-L	21	1-L
10	+5 V	22	SHIELD
11	8000-L	23	4000-L
12	2000-L	24	1000-L

Note:

(a) The *1 mark indicates that the pin is not in use.

(b) "-H" indicates high true and "-L" indicates low true.

(2) Connectors

(a) 9302-LV side : 57GE-40240-751 (DDK)

(b) Cable side : 57-30240 (DDK)

(3) Test start signal (AUXX, AUXY, or AUXZ)

- Always low true
- Required signal pulse : 1 ms
- Select 1 signal among AUXX, AUXY, and AUXZ with DIP switch SW3.

(4) Wait (WAIT) signal

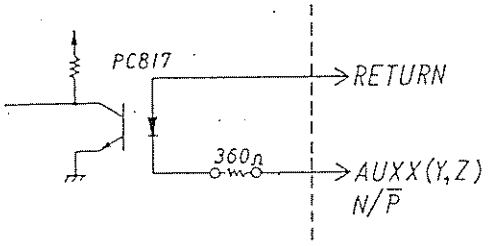
- Always low true
- It is output from when the 9302-LV starts testing to when it stops testing.

(5) Data signal (1 to 8000)

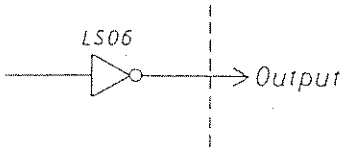
- Always low true
- It is used to output a ΔV_{BE} value.
- The signal is output as soon as a wait signal is canceled and is held till the test result change.

(6) Interface circuits

(a) Input circuits (AUXX, AUXY, AUXZ signal)



(b) Output circuits (Wait signal, data signals 1 to 8000)
A pull-up resistor is not inserted in each circuit.



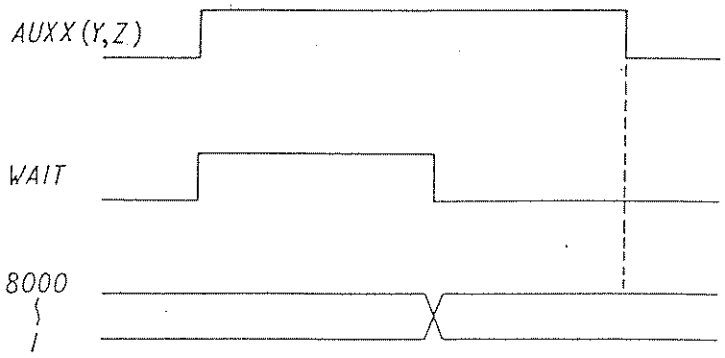
(7) DIP switch setting

Select a desired test start signal type with the DIP switch SW3 in the rear panel of the 93024-LV.

SW3	
SW No.	ON
1	AUXX
2	AUXY
3	AUXZ

Note : One desired switch only must be turned ON and 2 other switches must be turned OFF.

(8) Timing chart



1.11.5 SERIAL Connectors (A) and (B) (RS-232-C)

(1) Pin arrangement

SERIAL (A), (B) DB-25PT-N-S1 (JAE) Male			
Pin No.	Signal	Pin No.	Signal
1	FG (SHIELD)	14	–
2	TXD	15	–
3	RXD	16	–
4	RTS*1	17	–
5	CTS*1	18	–
6	(DSR)	19	–
7	SG	20	(DTR)
8	–	21	–
9	–	22	–
10	–	23	–
11	–	24	–
12	–	25	–
13	–		

*1 : Applicable to SERIAL (A) connector only

(a) SERIAL (A) connector
RTS and CTS signals are usable.
DSR and DTR signals are not usable.

(b) SERIAL (B) connector
RTS and CTS signals are not usable.
DSR and DTR signals are not usable.

(2) Connectors

(a) 9302-LV side : DB-25PT-N-S1 (JAE)
Two lock screws (#4-40) are used.

(b) Cable side : DB-25S-N (JAE) or equivalent

(3) DIP switch setting

Baud rate setting is made by the DIP switch SW1 in the rear panel of the 9302-LV.

SW1	
SW No.	ON
1	SERIAL (A) Baud Rate = 19200 bps
2	SERIAL (A) Baud Rate = 9600 bps*2
3	SERIAL (B) Baud Rate = 19200 bps
4	SERIAL (B) Baud Rate = 9600 bps*2
5	–
6	–

*2 : Baud rate is set at 9600 bps for both SERIAL (A) and SERIAL (B) connectors at the time of shipment, with the switches No.2 and No.4 turned ON.

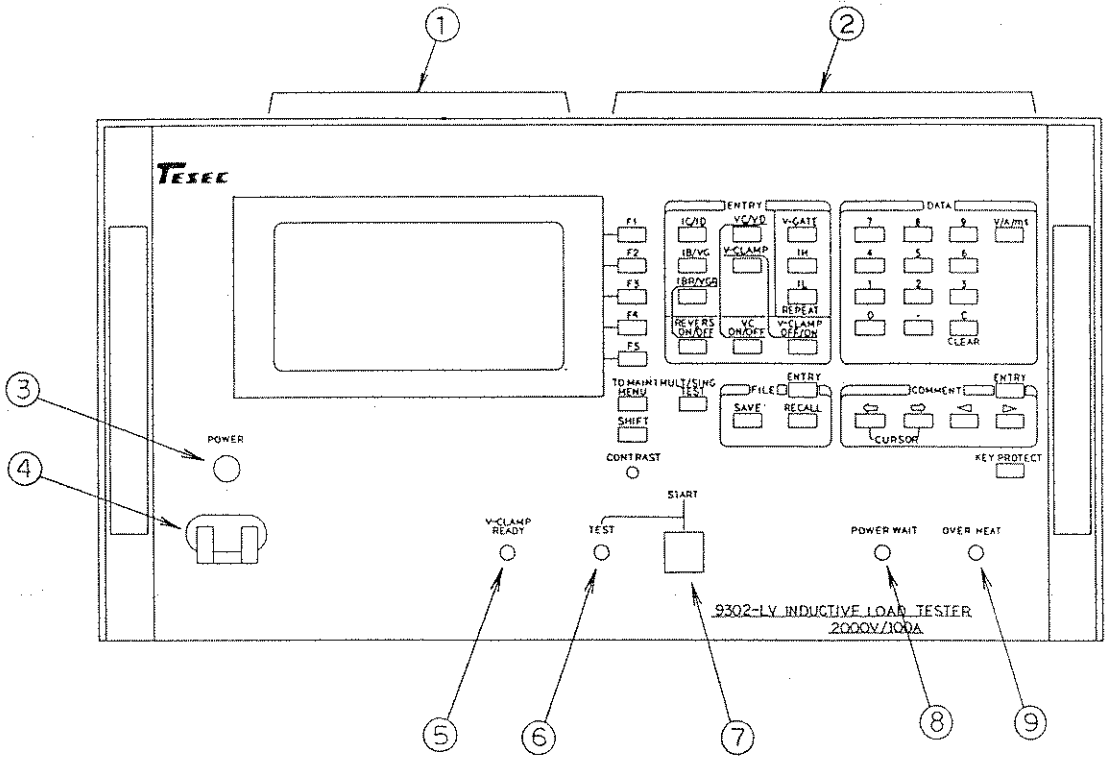
1.12 Power Requirements and Physical Characteristics

Model	9302-LV	9303-PU	9304-HB
Power supply	100 V ± 5 % AC, 50/60 Hz		
Power consumption	1 KVA		
Dimensions (mm)			
Width	431	431	240
Height	235	235	255
Depth	510	510	520
Weight (kg)	40	40	15

* Plug : 3-prong straight with ground

2. MANES AND FUNCTIONS OF MAIN PARTS

2.1 Front Panel of 9302-LV



(1) LCD — Displays test conditions, test result, judgements, etc.

(2) Key panels — The ENTRY keys are used to select set conditions and the DATA keys are used to input data.

(3) POWER indicator — Lights while the POWER switch is on.

(4) Power switch — Turns on/off power supply to the 9302-LV.

(5) V-CLAMP READY indicator

Lights when the collector clamp voltage reaches the set value. When the indicator is off, the START switch is invalid and the 9302-LV waits the operation.

(6) TEST indicator — Lights while a device is tested.

(7) START — Is validated when the front panel is selected in the START1 menu. By pushing the START switch, testing of a device starts.

(8) POWER WAIT indicator

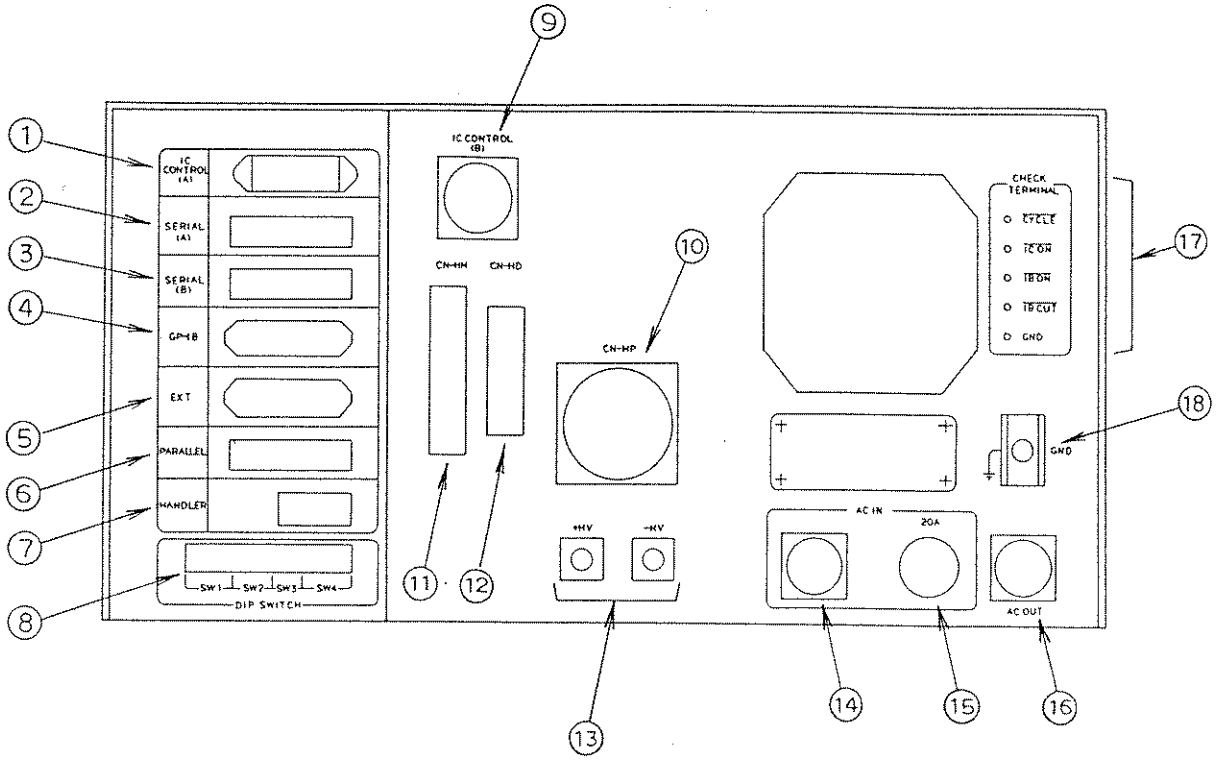
Turns on when each power supply voltage decreases to the specified value and turns out when the voltage increases to the specified value.

When the indicator is on, the START switch is invalid and the 9302-LV waits the operation.

(9) OVERHEAT indicator

Lights when the temperature of the heat sink for the power inside the 9303-PU exceeds 60°C. The 9302-LV waits the operation. When the temperature decreases to 60°C or below, the operation starts automatically.

2.2 Rear Panel of 9302-LV



(1) IC CONTROL(A) Connects the WT9316 logic cable to the 9303-PU power unit.

(2) SERIAL (A) Is the RS-232-C interface connector for interfacing a personal computer

(3) SERIAL (B) Is the standby RS-232-C interface connector. (spare)

(4) GP-IB Is the GP-IB interface connector.

(5) EXT Is the external interface connector for receiving a test start signal and outputting a test result.

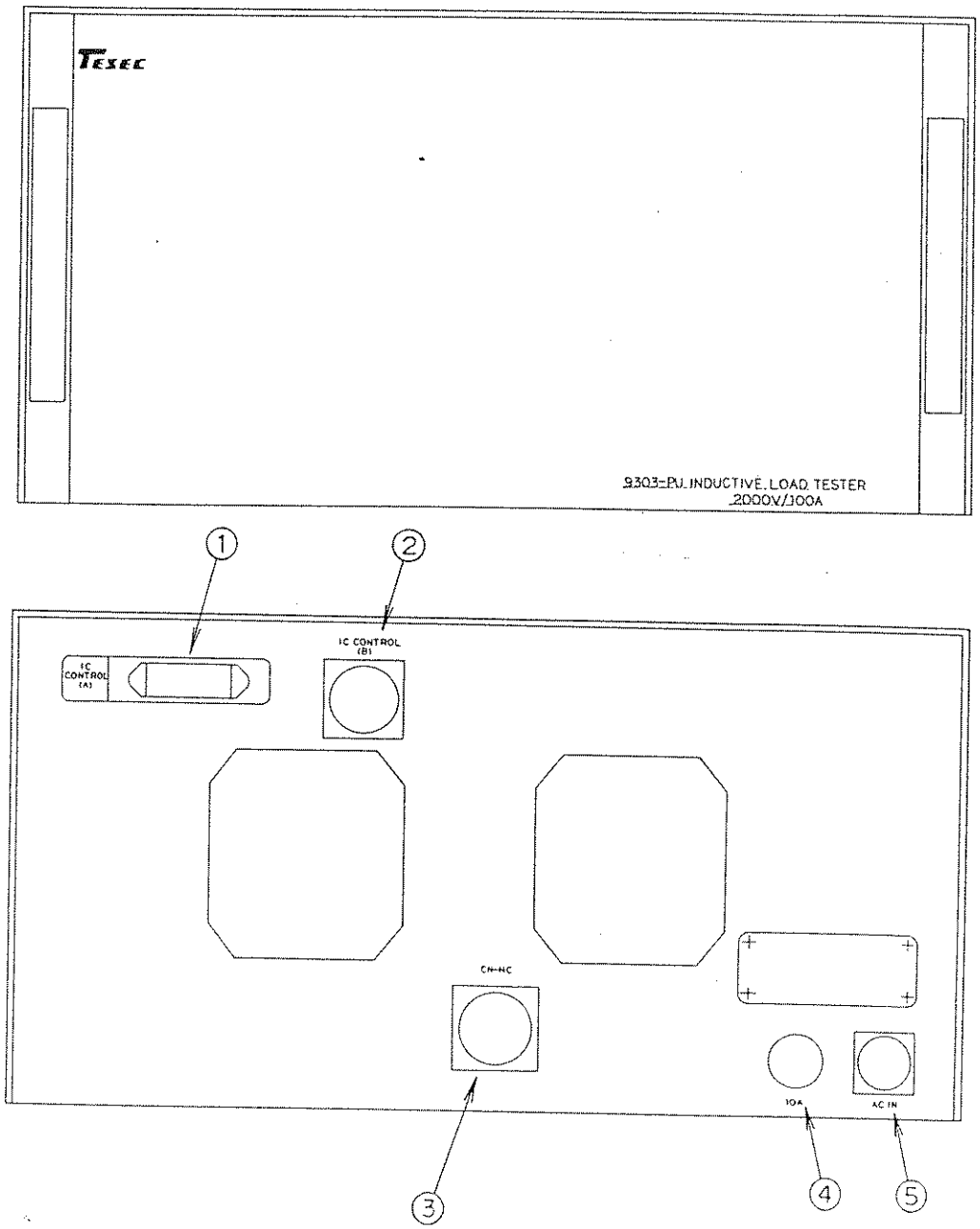
(6) PARALLEL Is the Centronics interface connector for interfacing a printer.

(7) HANDLER Is the handler interface connector.

(8) DIP SWITCH Is for the DIP switches which set the conditions for the SERIAL (A), GP-IB, EXT, and HANDLER connectors.

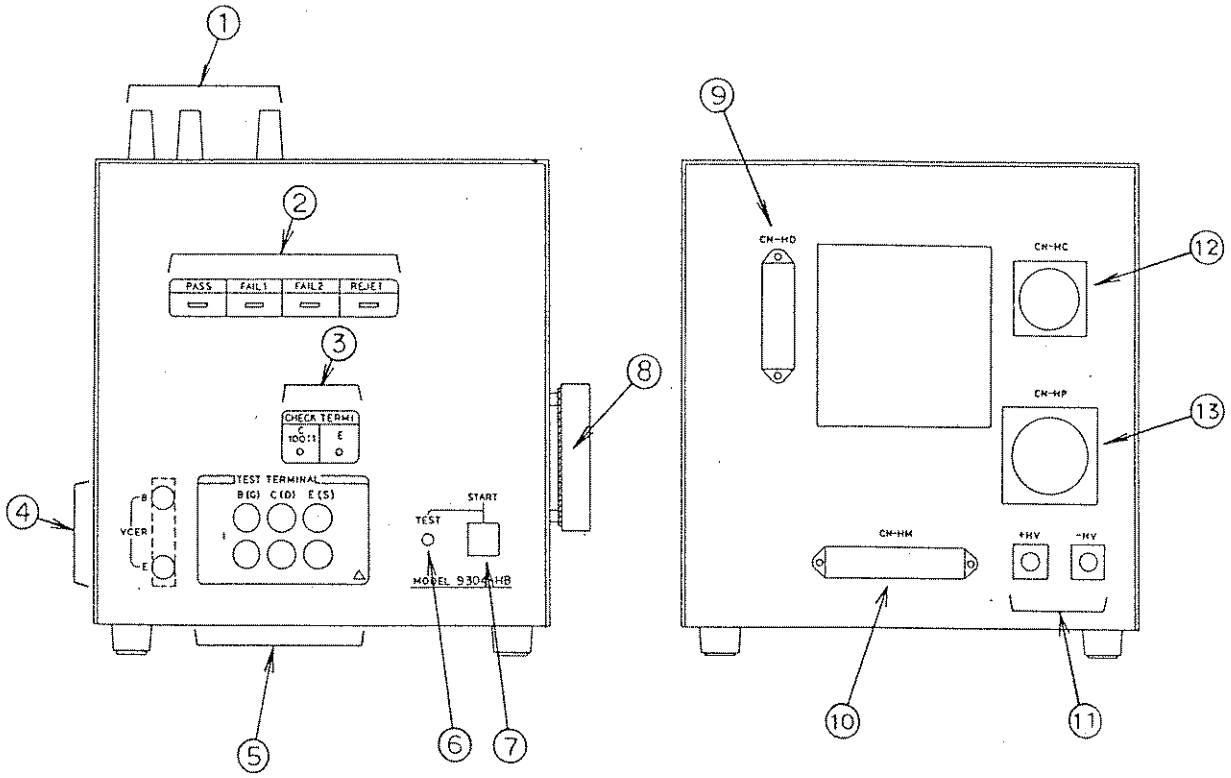
(9) IC CONTROL (B)	Connects the WT9313 logic cable to the 9303-PU power unit.
(10) CN-HP	Is for the AC power supply connector for connecting the WT9311 power cable to the 9304-HB test head.
(11) CN-HM	Is for the relay control connector for connecting the WT9314 logic cable to a 9304-HB test head.
(12) CN-HD	Is for the DETECTOR board control connector for connecting the WT9315 logic cable to a 9304-HB test head.
(13) +HV, -HV	Are for the collector-clamp high voltage connectors. Wait surely for 3 minutes after power off and then connect or disconnect cables. Connects WT9317 BNC cables to the test head 9304-HB.
(14) AC IN	Is the AC power input connector for connecting the WN8610 AC power cable.
(15) 20 A	Is the fuse holder of a 20 A fuse.
(16) AC OUT	Is the AC power output connector for connecting the WN8511 power cable to the 9303-PU power unit.
(17) CHECK TERMINAL	Is for the check terminals.
(18) GND	Is the ground terminal.

2.3 Front and Rear Panels of 9303-PU



(1)	IC CONTROL(A)	Connects the WT9316 logic cable to the 9302-LV.
(2)	IC CONTROL(B)	Connects WT9313 logic cable to the 9302-LV.
(3)	CN-HC	Is for the IC output connector for connecting the WT9312 cable to the 9304-HB test head.
(4)	10 A	Is the fuse holder for a 10 A fuse.
(5)	AC IN	Is the AC power input connector for connecting the WT8511 power supply cable from the 9302-LV.

2.4 Front, Rear, and Right Side Panels of 9304-HB



(1)	Coil connect terminals	Is connected with a coil.
(2)	Test result indicators	Indicates the test result in 4-bin mode.
(3)	CHECK TERMI	Are the check terminals for an oscilloscope. Outputs by 0 ~ ±20 V (100:1).
(4)	B-E terminals	Is the B-E terminals for measurement of V_{CER}. Attach a resistor.
(5)	TEST TERMINAL	Are used when a test fixture is used for testing.
(6)	TEST indicator	Lights while a device is tested.
(7)	START	Is validated when HB is selected in the START1 menu. By pushing the START switch, testing of a device starts.

(8) CURRENT TERMINAL Are for a current probe.

(9) CN-HD Is for the DETECTOR board control connector for connecting the WT9315 logic cable.

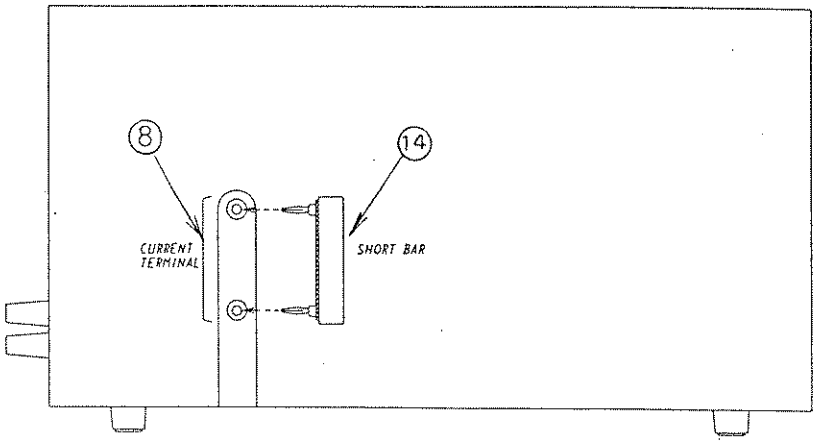
(10) CN-HM Is for the relay control connector for connecting the WT9314 logic cable.

(11) +HV, -HV Are for the collector-clamp high voltage connectors. Wait surely for 3 minutes after power off, and then connect or disconnect cables.

(12) CN-HC Is for the IC output connector for connecting the WT9312 cable.

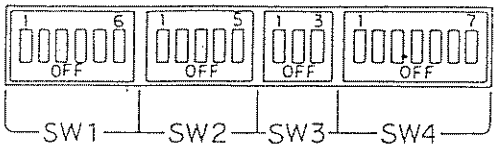
(13) CN-HP Is for the AC power supply connector for connecting the WT9311 power cable.

(14) SHORT BAR Shall be surely used for short when the connect terminals are not used.



3. OPERATION PREREQUISITES

3.1 DIP Switch Setting (Rear Panel of 9302-LV)



(1) SW1

Sets the baud rates of the SERIAL connector.

SW No.	ON
1	SERIAL (A) Baud Rate = 19200 bps
2	SERIAL (A) Baud Rate = 9600 bps
3	SERIAL (B) Baud Rate = 19200 bps
4	SERIAL (B) Baud Rate = 9600 bps
5	–
6	–

(2) SW2

Sets the address of the GP-IB connector.

SW No.	ON
1	GP-IB Address 1(LSB)
2	GP-IB Address 2
3	GP-IB Address 3
4	GP-IB Address 4
5	GP-IB Address 5 (MSB)

(3) SW3

Selects a start signal type of the EXT connector.

SW No.	ON
1	EXT AUXX
2	EXT AUXY
3	EXT AUXZ

(4) SW4

Set logic (high true and low true) for signal of the HANDLER connector.

SW No.	ON	OFF
1	SORT-H	SORT-L
2	END-H	END-L
3	START-L	
4	(No. 5,6 = OFF)	
5	START-H	
6	(No. 3,4 = OFF)	
7	–	–

Note :

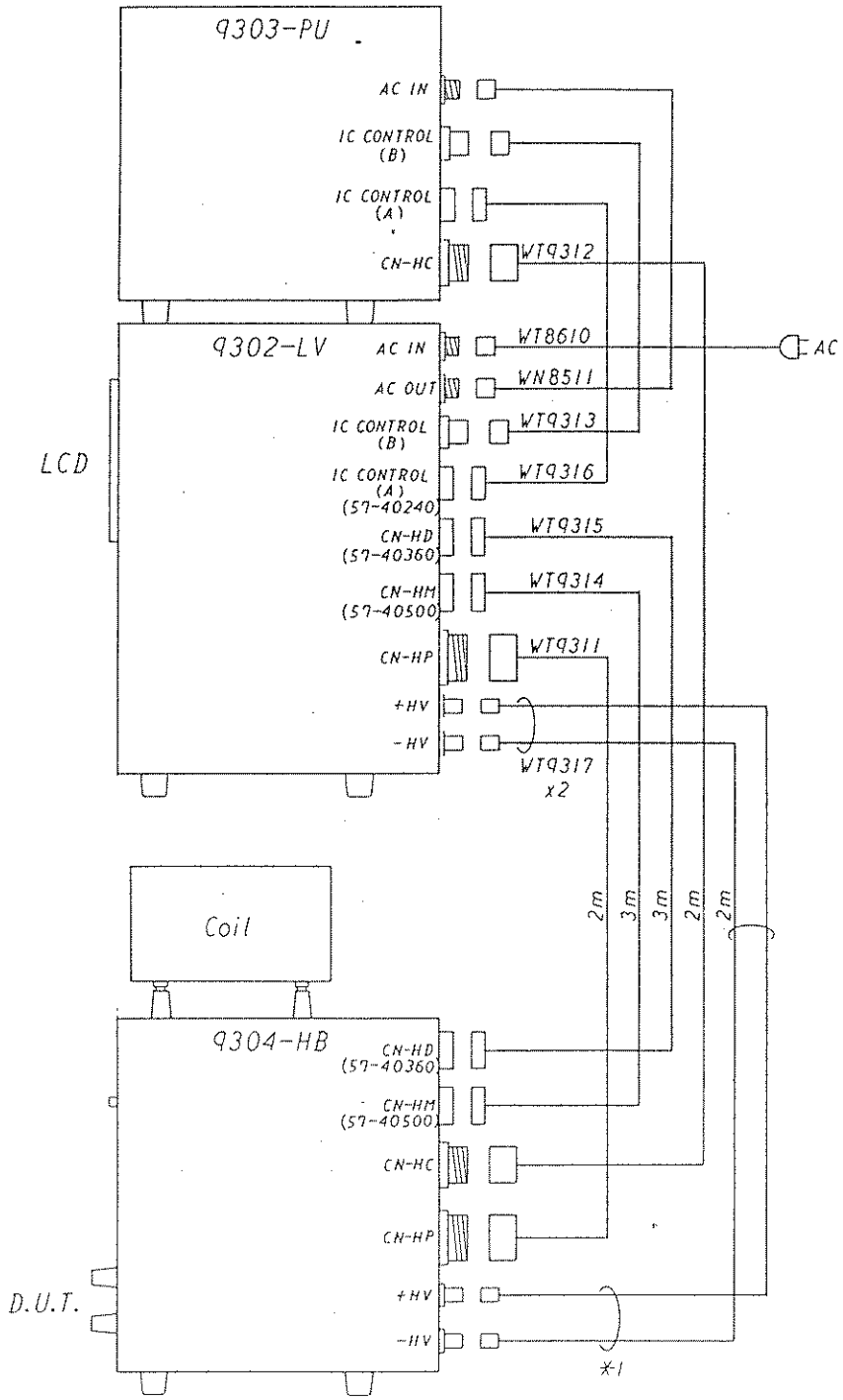
(a) SORT = PASS, FAIL

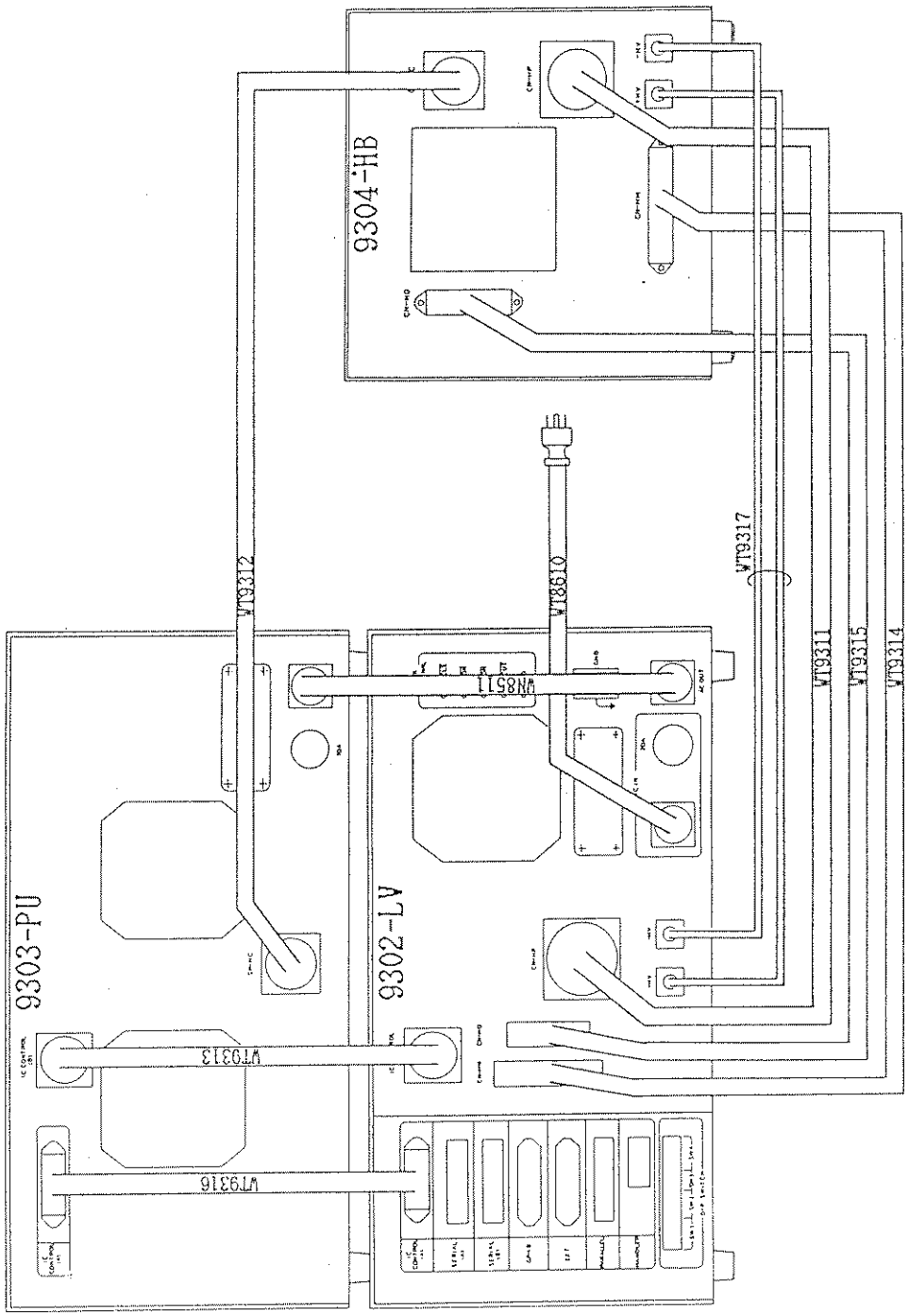
PASS, FAIL1, FAIL2, REJECT

(b) -H indicates high true and -L indicates low true.

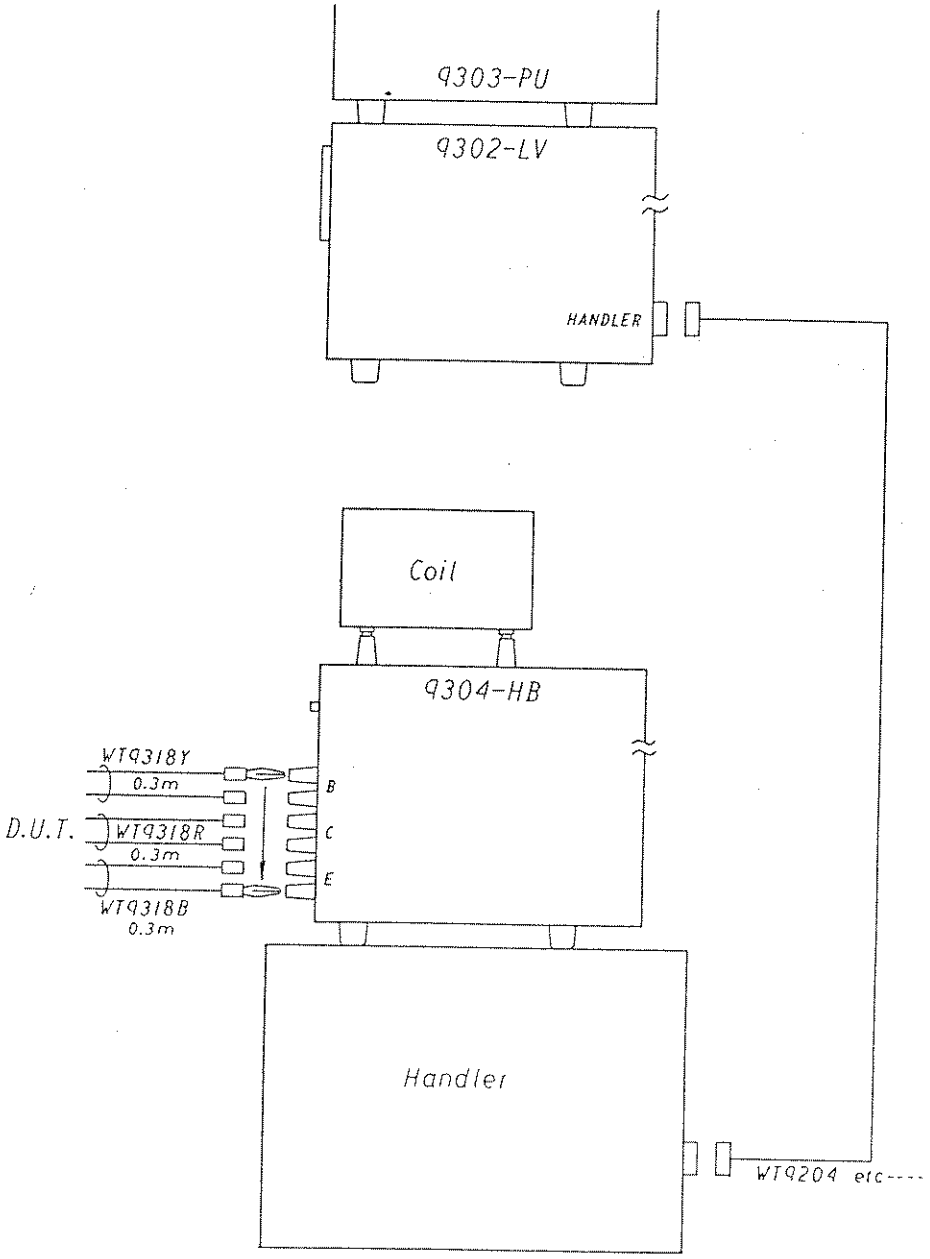
3.2 Cable Connections

3.2.1 Connecting 9302-LV, 9303-PU, and 9304-HB



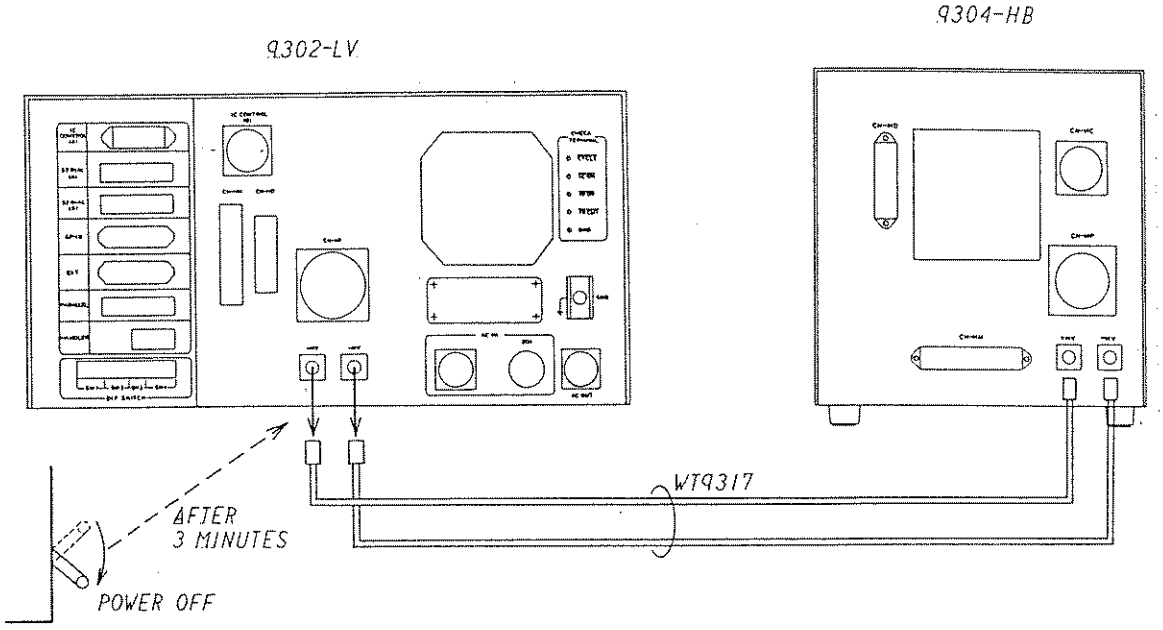

9304-HB
9303-PU
9302-LV
WT9312
WT9313
WT9316
WT8810
WT9317
WT9311
WT9315
WT9314
WN8511

3.2.2 Connecting 9302-LV to Handler



3.2.3 Connecting or Disconnecting Cable

- Wait for 3 minutes after power off and then connect or disconnect the cables connected to +HV and -HV connectors.
- Pay attention when connecting the cables to the +HV and -HV connectors. If its polarity is wrong , a trouble will occur.
- Connect or disconnect all cables after power off.



3.2.4 Fitting Board Retainer

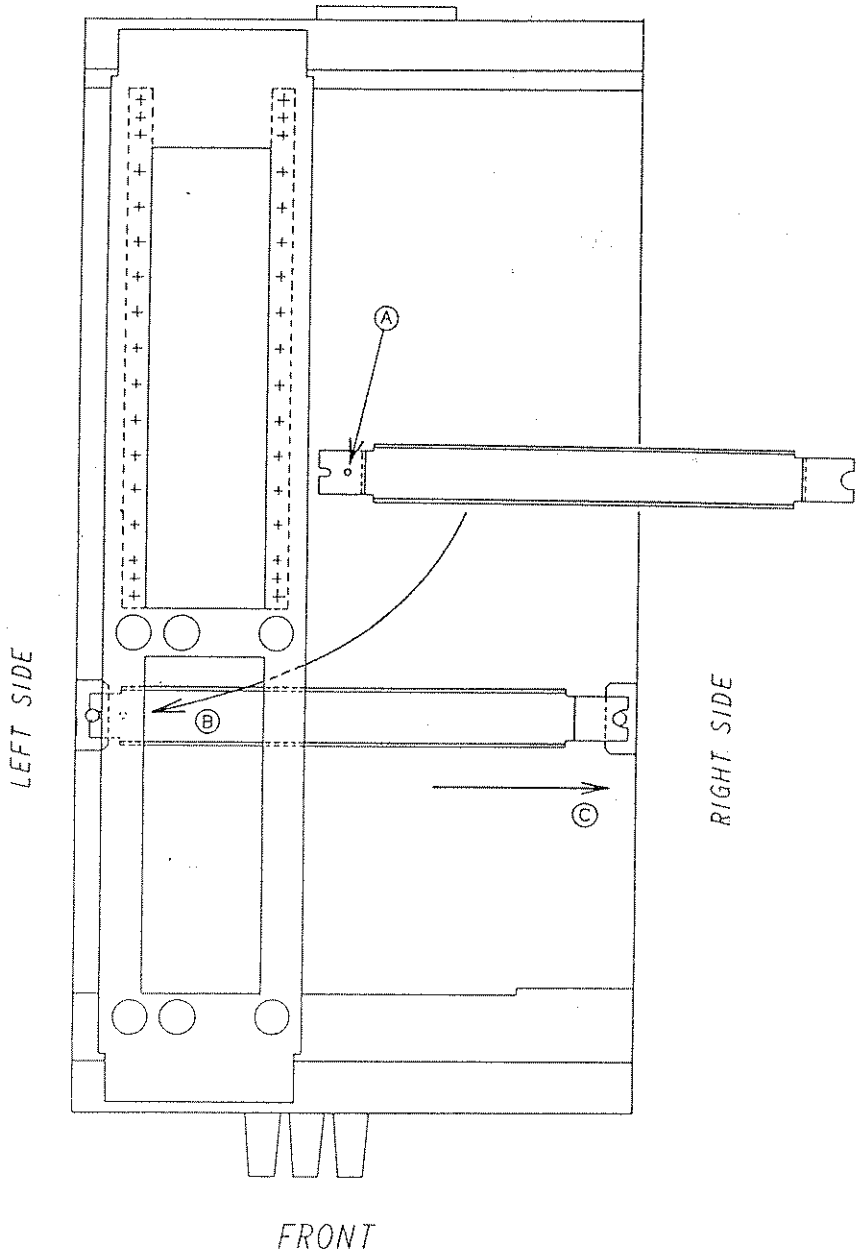
(1) Place the board retainer by positioning the fix hole (A) at the left side as shown below.

(2) Insert the board retainer under the coil fix plate. (B)

(3) Pull fully the board retainer to the right side while the board retainer is installed. (C)

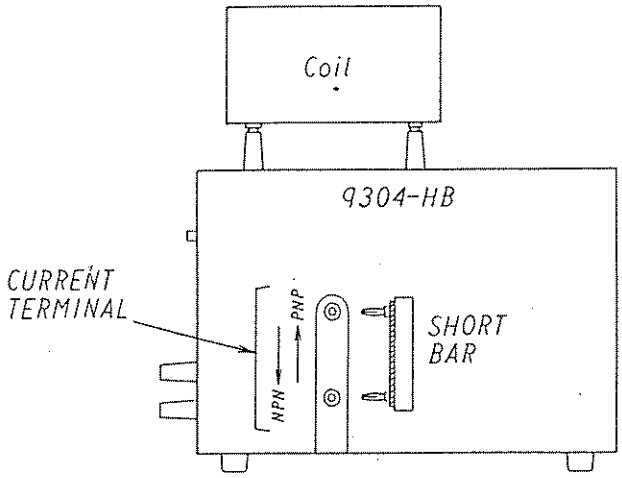
(4) Fix the screws.

(5) Take care not to take away the screws when the board retainer is removed.



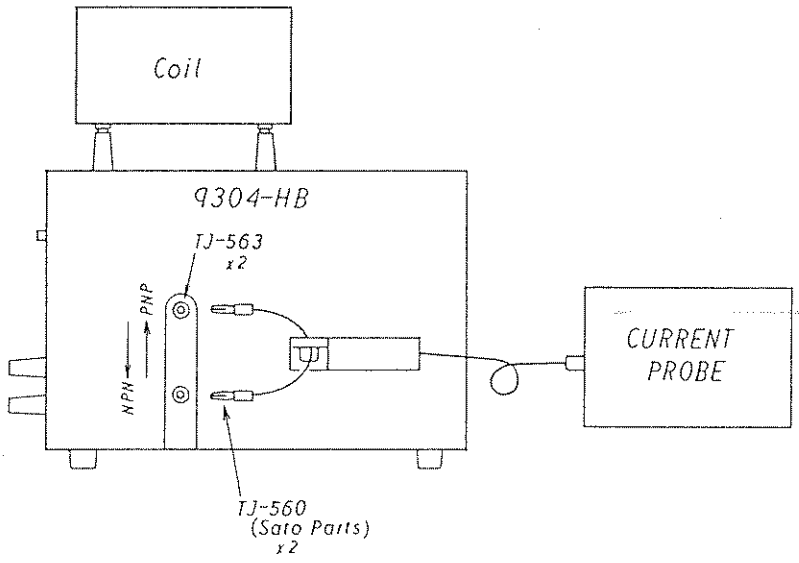
3.2.5 Usage of Current Terminal

(1) Remove the short bar.



(2) Solder a cable which is suitable for the banana plugs, and connect it to the sockets as shown below.

(3) Set the current probe.



(4) Short surely with the short bar when the current probe is not used.

4. MAINTENANCE

4.1 I_C Accuracy

Carry out the following steps to check the calibration of I_C.

(a) Set the V-CLAMP to OFF.

(b) Short the coil terminals.

(c) Connect a resistor of 0.1 Ω in series between C and E.

(d) Set I_C at any desired value.

(e) Get a reading of voltage (CH1-CH2) across the resistor with an oscilloscope.

(f) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

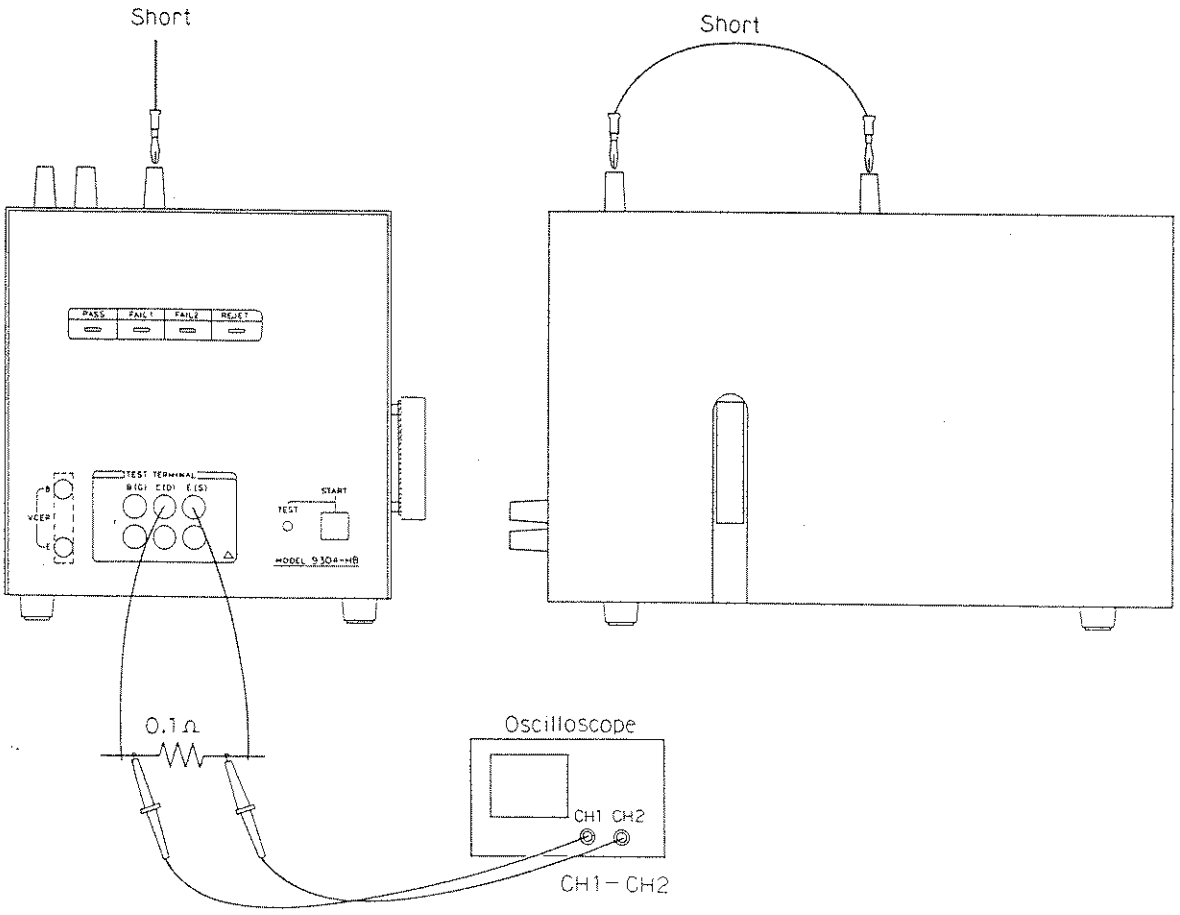
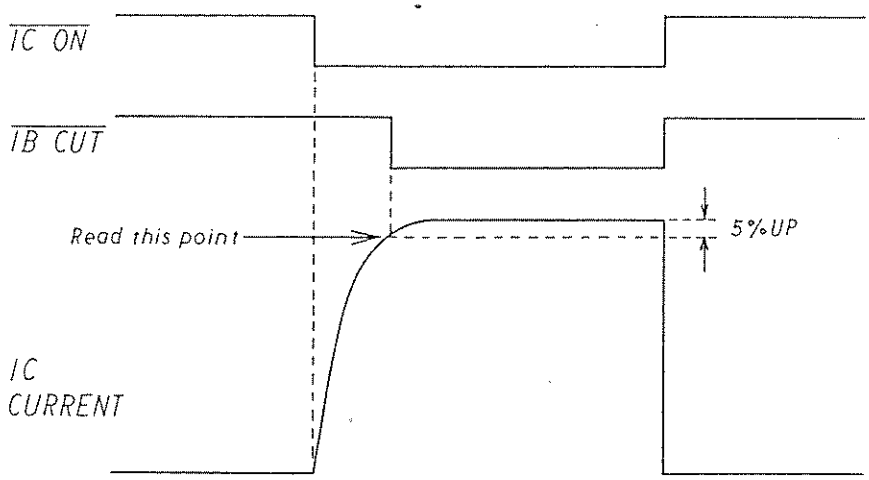


Figure 4.1

(g) Connect a probe of the oscilloscope to the check terminal $\overline{\text{IB CUT}}$ and get a correct reading of I_C current value by referring to the timing chart below.



4.2 I_B Accuracy

Carry out the following steps to check the calibration of I_B.

(a) Set the V-CLAMP to OFF.

(b) Set the polarity to N-FET or P-FET.

(c) Open the coil terminals and the C-E line.

(d) Short B and E.

(e) Set I_B at any desired value.

(f) Set a current probe as shown in Figure 4.2 and get a reading of current waveform with an oscilloscope.

(g) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

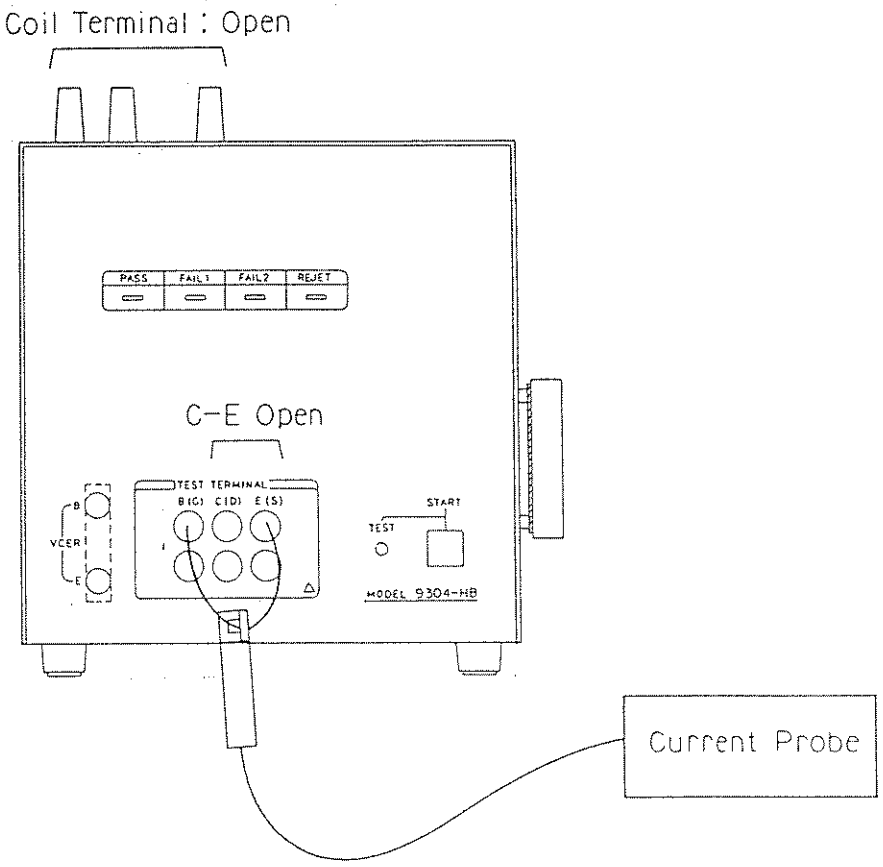


Figure 4.2

4.3 V_G Accuracy

Carry out the following steps to check the calibration of V_G.

(a) Set the V-CLAMP to OFF.

(b) Set the polarity to N-FET or P-FET.

(c) Open the coil terminals and the C-E line.

(d) Set V_G at any desired value.

(e) Get a reading of voltage waveform at the B(G) terminal with an oscilloscope.

(f) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

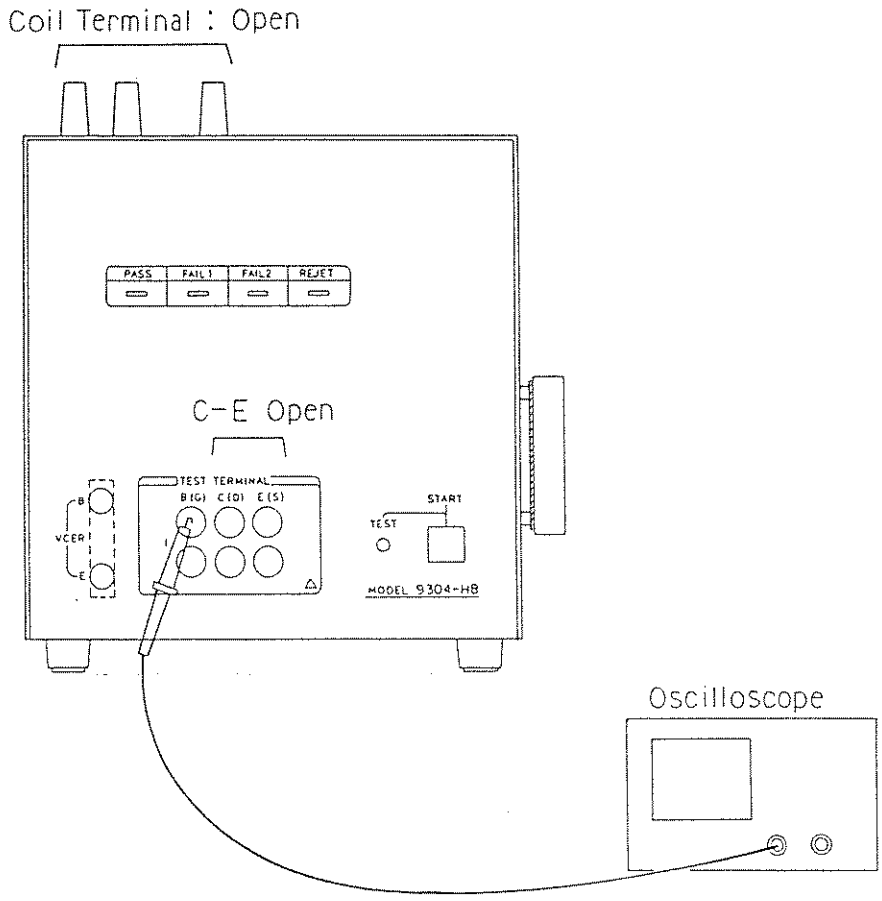


Figure 4.3

5. OSCILLATION SUPPRESSION

5.1 Handler Interface

(1) Transistor

Put 10~20 pcs of cores (T314 OP4 3.2-2H) at the nearest position to the base terminal of a device.

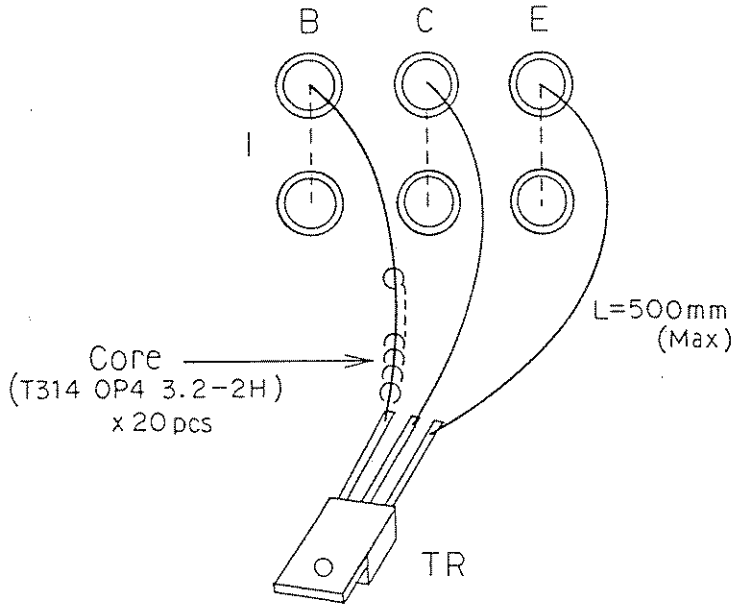


Figure 5

6. ADJUSTMENT

6.1 I_C Calibration

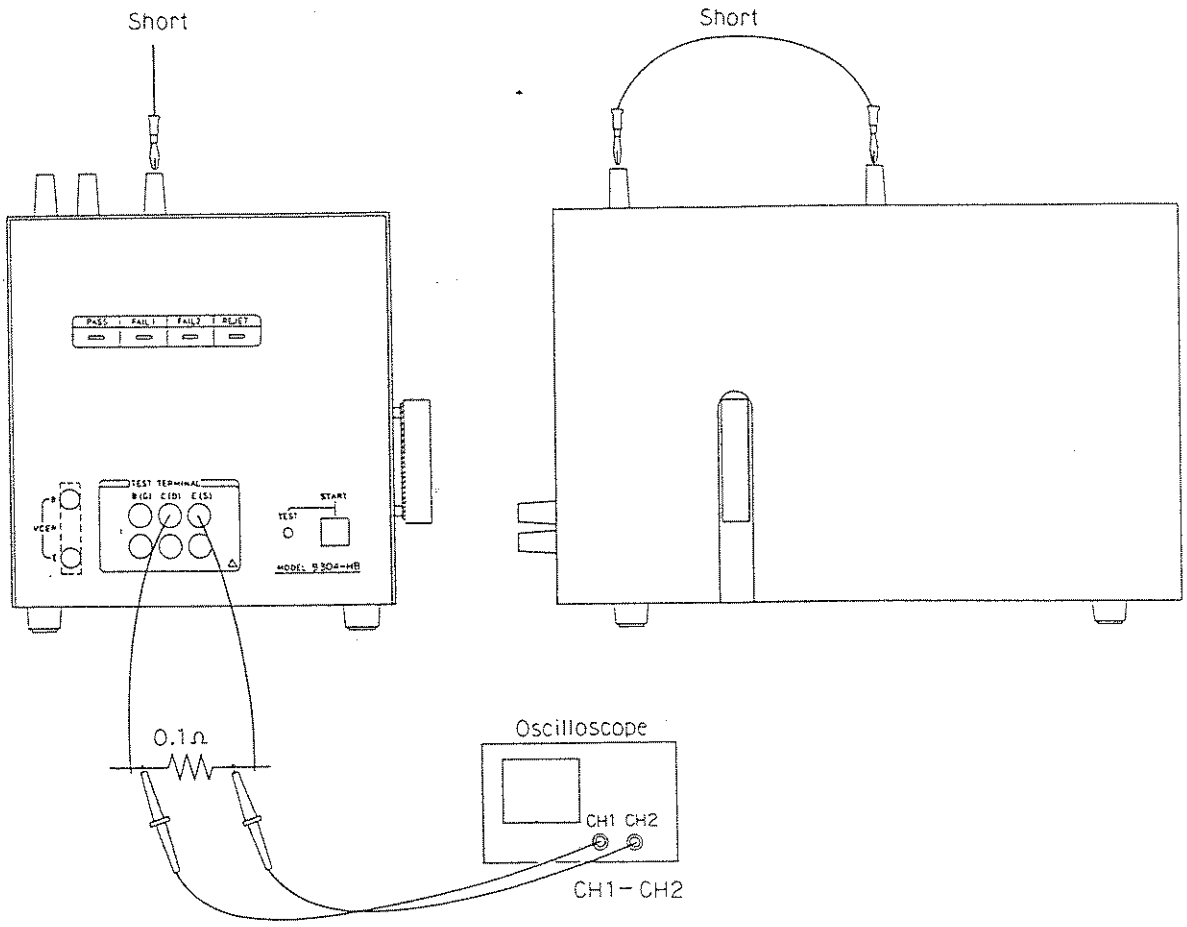


Figure 6.1

6.1.1 I_C Calibration Procedure

Carry out the following steps to check the I_C calibration.

(a) Set the polarity to N-TR. or P-TR.

(b) Short the coil terminals.

(c) Connect a resistor (0.1 Ω) in series between C and E.

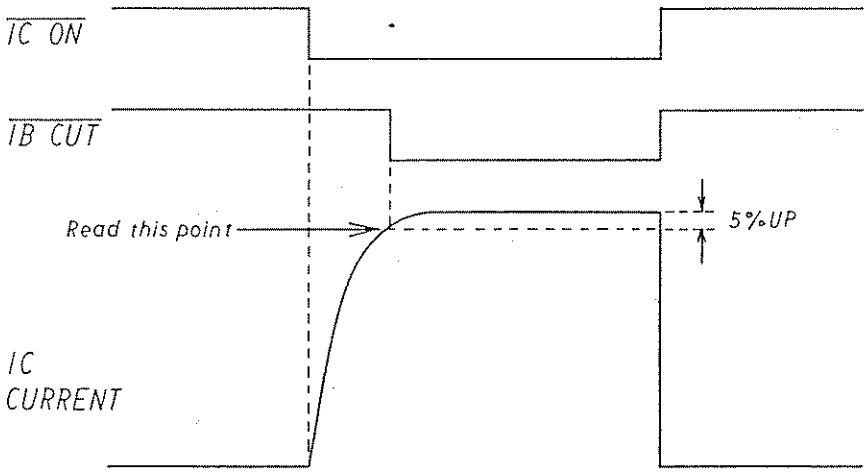
(d) Set I_C at any desired value.

(e) Get a reading of voltage (CH1-CH2) across the resistor with an oscilloscope.

(f) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

Item	Measurement Range	Accuracy	Resolution
IC	1.0 – 100.0 A	±(2% + 0.4 A)	0.1 A

(g) Connect a probe of the oscilloscope to the check terminal $\overline{\text{IB CUT}}$ and get a correct reading of I_C current value by referring to the timing chart below.



6.1.2 When No I_C is Applied

Check on the following points.

(a) IE GEN board (PT9333) in the 9303-PU

Whether the analog switch ASW1 which controls the input of the OP2 op-amp works properly with the $\overline{\text{IC ON}}$ signals.

(b) P-WAIT lamp

- Whether the P-WAIT lamp is lit up. If it is lit up, immediately turn off the power supply and check for the power transistor module on the heatsink of the 9303-PU.
- Open each power supply output and check for the power supply.

6.1.3 When Exact Value of I_C As Preset is Not Applied

Open the coil terminals and the C-E line. Check the I_C GEN board (PT9333) on the following points.

(a) D/A Converter adjustment

(i) Connect a DVM between the check terminals TP6 and TP0.

(ii) Set the polarity to N-TR. and I_C to 0 A. Push the start switch and adjust the variable resistor VR4 to have the DVM read 0.00 mV (±0.1 mV).

(iii) Set the polarity to N-TR. and I_C to 100 A. Push the start switch and adjust the variable resistor VR3 to have the DVM read -5.000 V (±0.001 V).

(iv) Set the polarity to P-TR. and I_C to 100 A. Push the start switch and confirm that the DVM reads +5.000 V (±0.001 V).

(v) Repeat the steps (ii) to (iv) above until the desired readings are obtained.

(vi) Confirm that the exact value of I_C as programmed is applied with the range of 0 A to 100 A.

IC/VC (A)	Output (V)
0.0	0.00 m
0.1	∓5.00 m
0.2	∓10.00 m
0.4	∓20.00 m
0.8	∓40.00 m
1.6	∓80.00 m
3.2	∓160.0 m
6.4	∓320.0 m
12.8	∓640.0 m
25.6	∓1.280
51.2	∓2.560
100.0	∓5.000

(b) Offset adjustment of OP2 op-amp

(i) Connect a DVM between the check terminals TP4 and TP0.

(ii) Adjust the variable resistor VR2 to have the DVM read 0.00 mV (±0.1 mV).

(c) Offset adjustment of OP1 op-amp

(i) Connect a DVM between the check terminals TP1 and TP0.

(ii) Adjust the variable resistor VR1 to have the DVM read 0.00 mV (±0.1 mV).

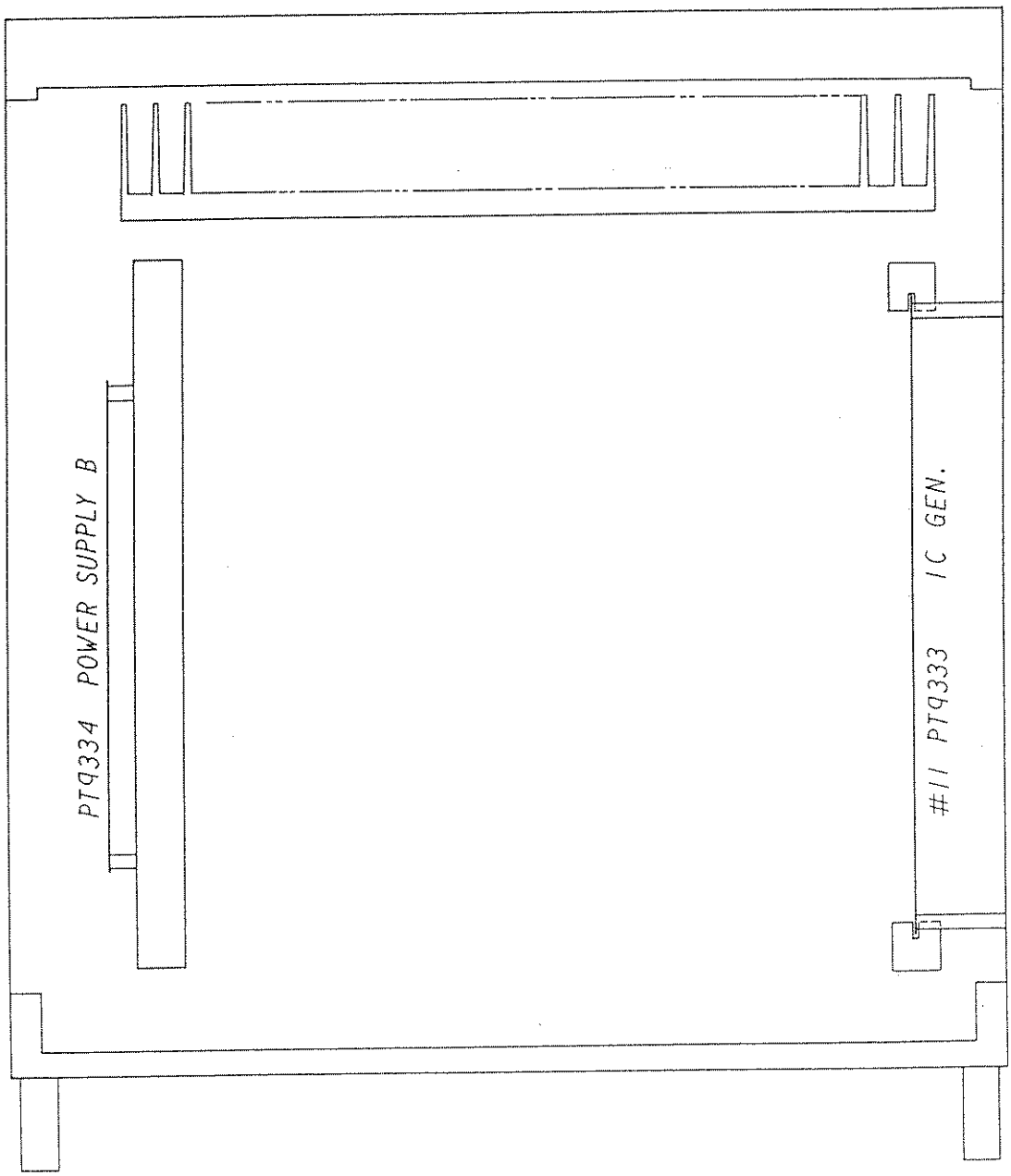


Figure 6.1b 9303-PU Top View

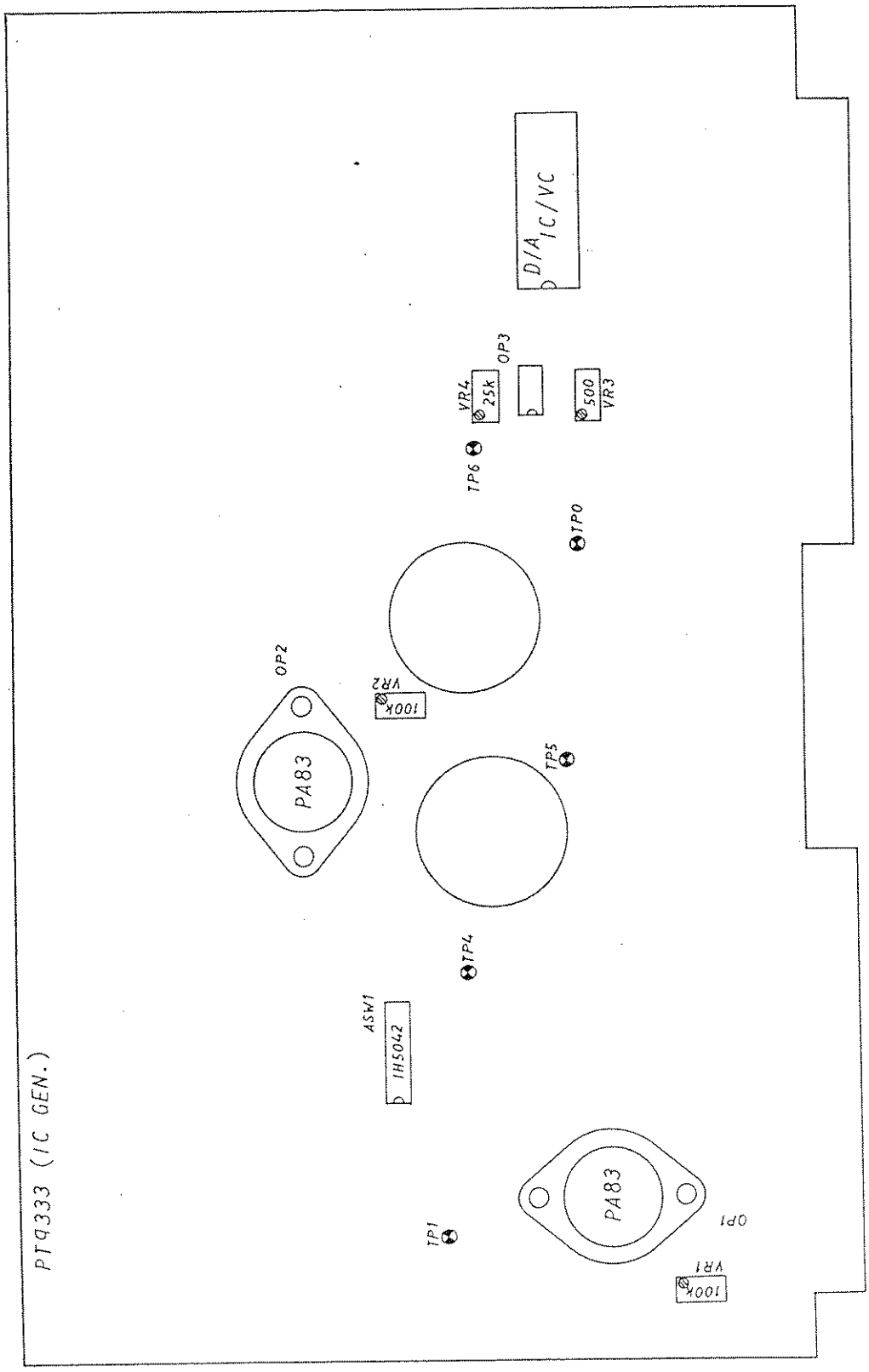


Figure 6.1c IC GEN Board (PT9333)

6.2 I_B Calibration

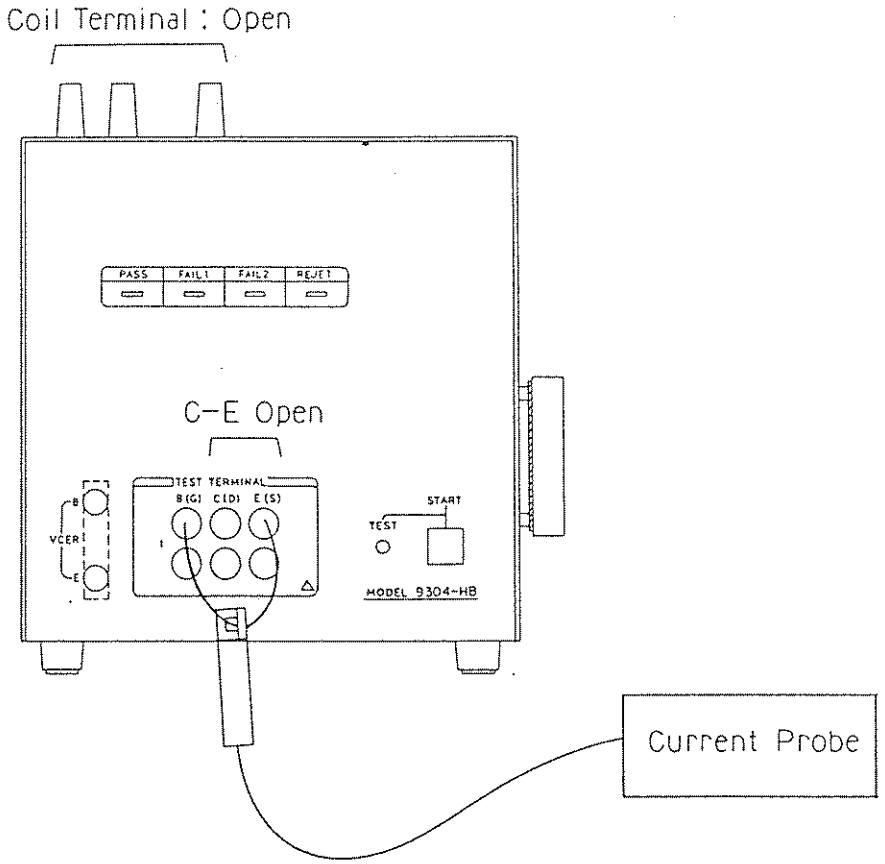


Figure 6.2a

6.2.1 I_B Calibration Procedure

Carry out the following steps to check the I_B calibration.

(a) Set the polarity to N-TR. or P-TR.

(b) Open the coil terminals and the C-E line.

(c) Short B and E.

(d) Set I_B at any desired value.

(e) Set a current probe as shown in Figure 6.2a and get a reading of current waveform with an oscilloscope.

(f) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

Item	Measurement Range	Accuracy	Resolution
IB IBR	0.01 ~ 20.00 A	±10%	0.01 A

6.2.2 When No I_B is Applied

Check the IB GEN board (PT9321) in the 9304-HB on the following points.

(a) Connect a DVM between the check terminals TP1 and TP0. Confirm that the DVM reads +20.00 V (±0.2 V).

(b) Connect a DVM between the check terminals TP2 and TP0. Confirm that the DVM reads -20.00 V (±0.2 V).

6.2.3 When Exact Value of I_B As Preset is Not Applied

Check the RESISTOR board (PT9320) in the 9304-HB on the following points.

(a) Whether the relays of K3~K16 (K19~K32) function correctly.

IB (A)	Relay No.
0.01	K16 (K32)
0.02	K15 (K31)
0.04	K14 (K30)
0.08	K13 (K29)
0.16	K12 (K28)
0.32	K11 (K27)
0.64	K10 (K26)
1.28	K9 (K25)
2.56	K8, 7 (K23, 24)
5.12	K6, 5 (K21, 22)
10.24	K4, 3 (K19, 20)

(b) Turn off power supply and check whether or not each relay is shorted with a circuit tester.

(c) Confirm that the applied current is polarity-reversed. Short the coil terminals and the C-E line.

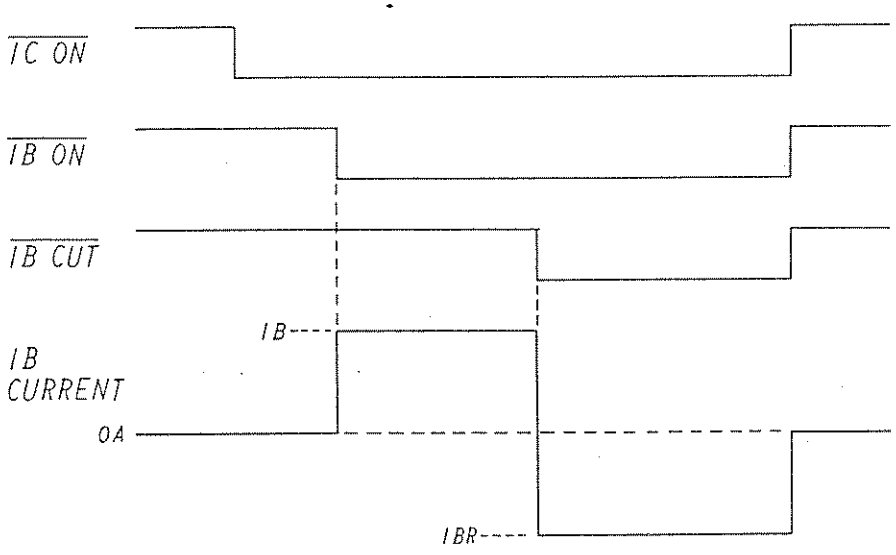
(i) Set the test conditions as follows:

N-TR/P-TR

IC = 0 A	VC = –	V-GATE = 0 V
IB = 0.01~20.00 A	V-CLAMP = –	IH = 0 A
IB = 0.01~20.00 A		IL = 0 A

(ii) Connect an oscilloscope to the check terminal $\overline{\text{IB CUT}}$ on the 9302-LV rear panel. Push the start switch and confirm that $\overline{\text{IB CUT}}$ signals are output.

(iii) Short B and E and set a current probe. Push the start switch and confirm that the current waveform shown in the timing chart below is obtained.



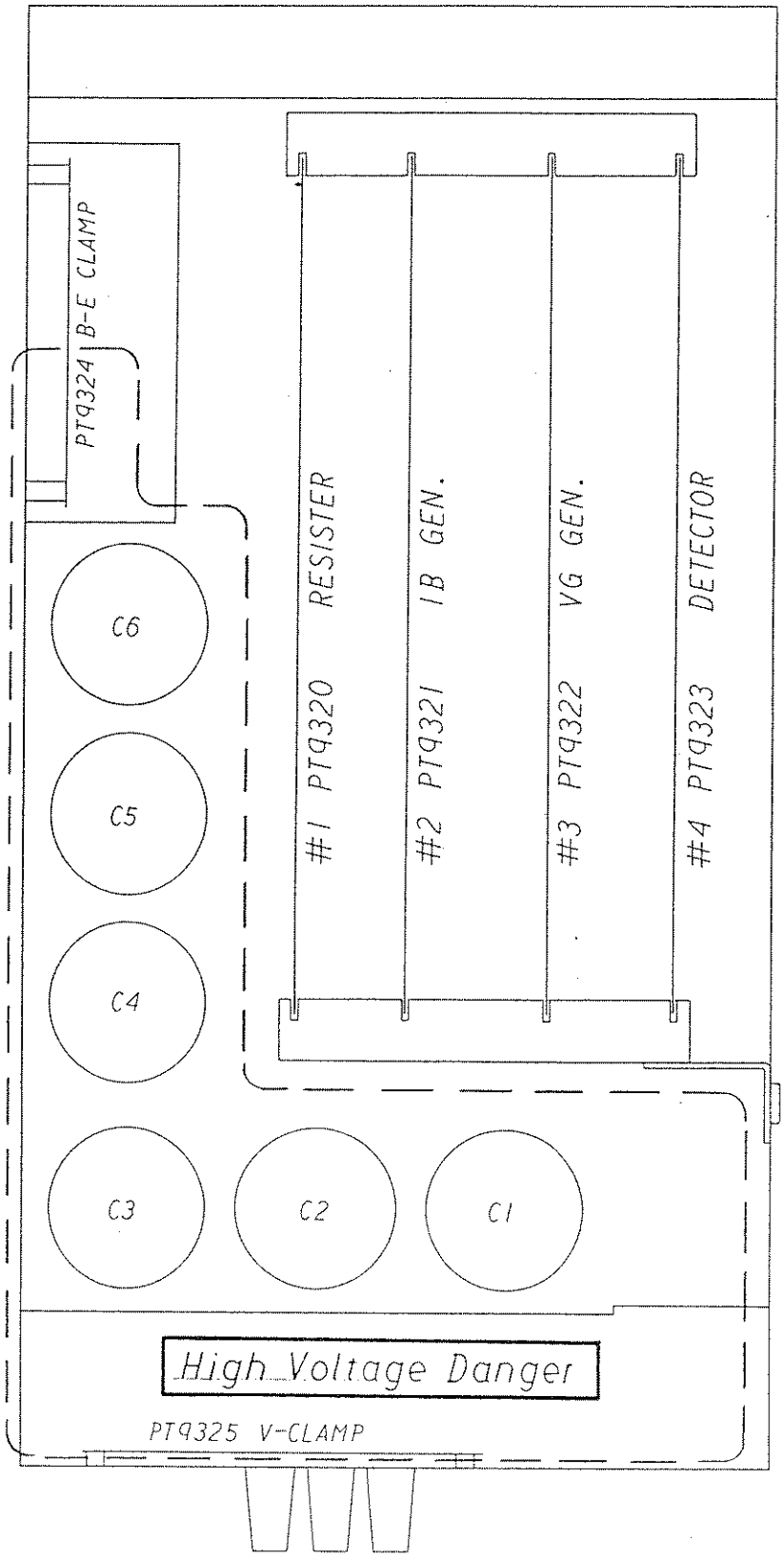


Figure 6.2b 9304-HB Top View

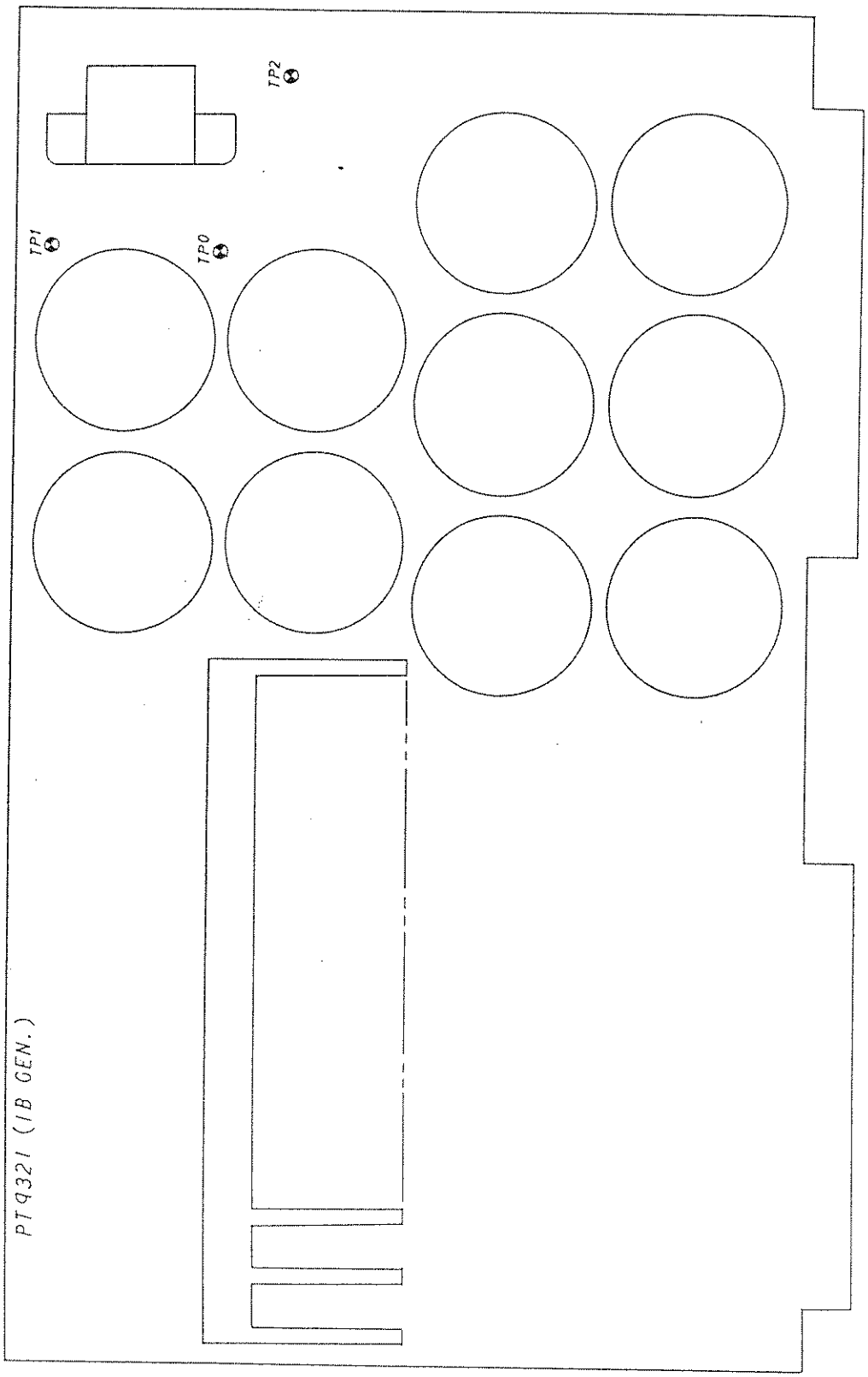


Figure 6.2c IB GEN Board (PT9321)

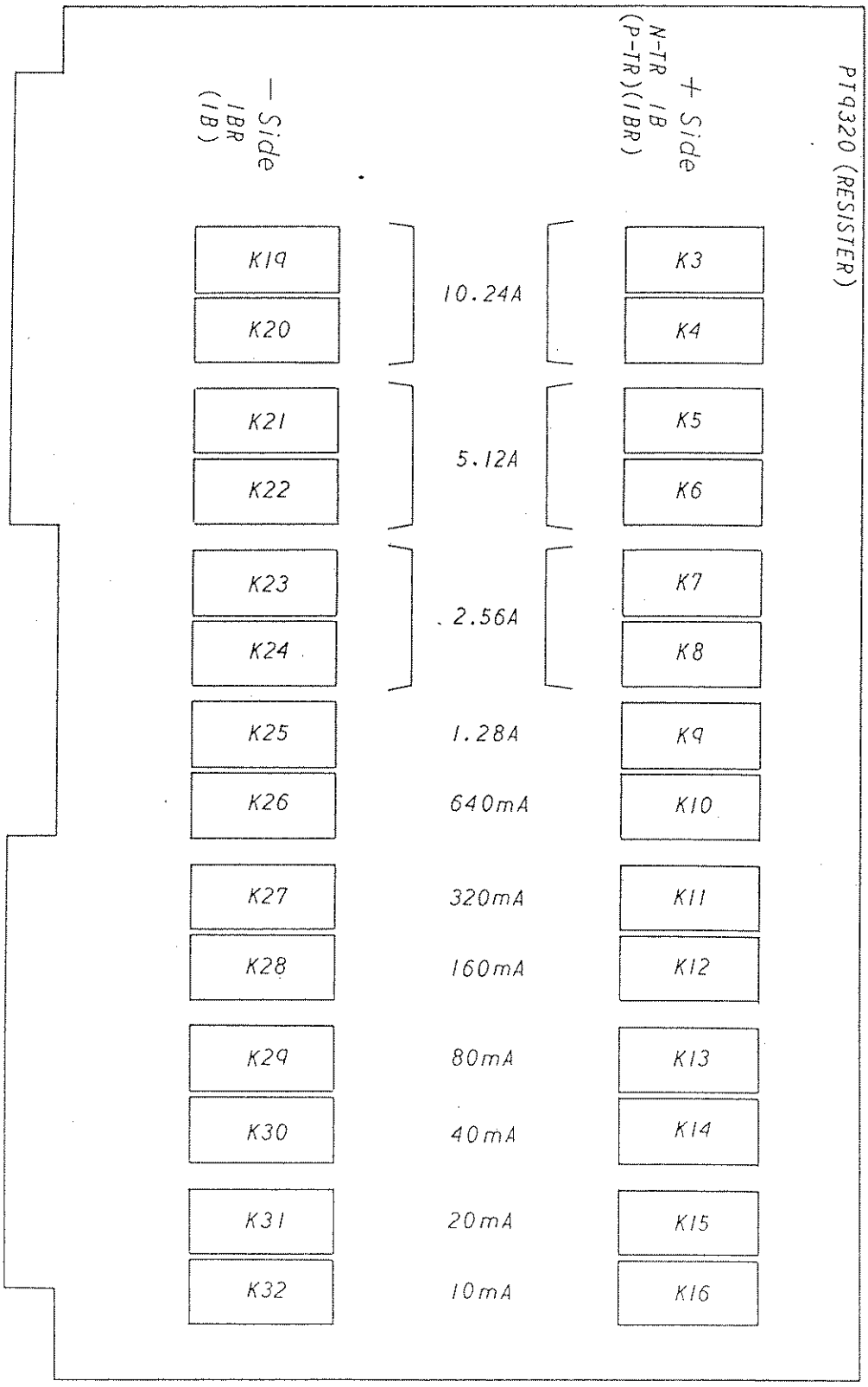


Figure 6.2d RESISTOR Board (PT9320)

6.3 V_G Calibration

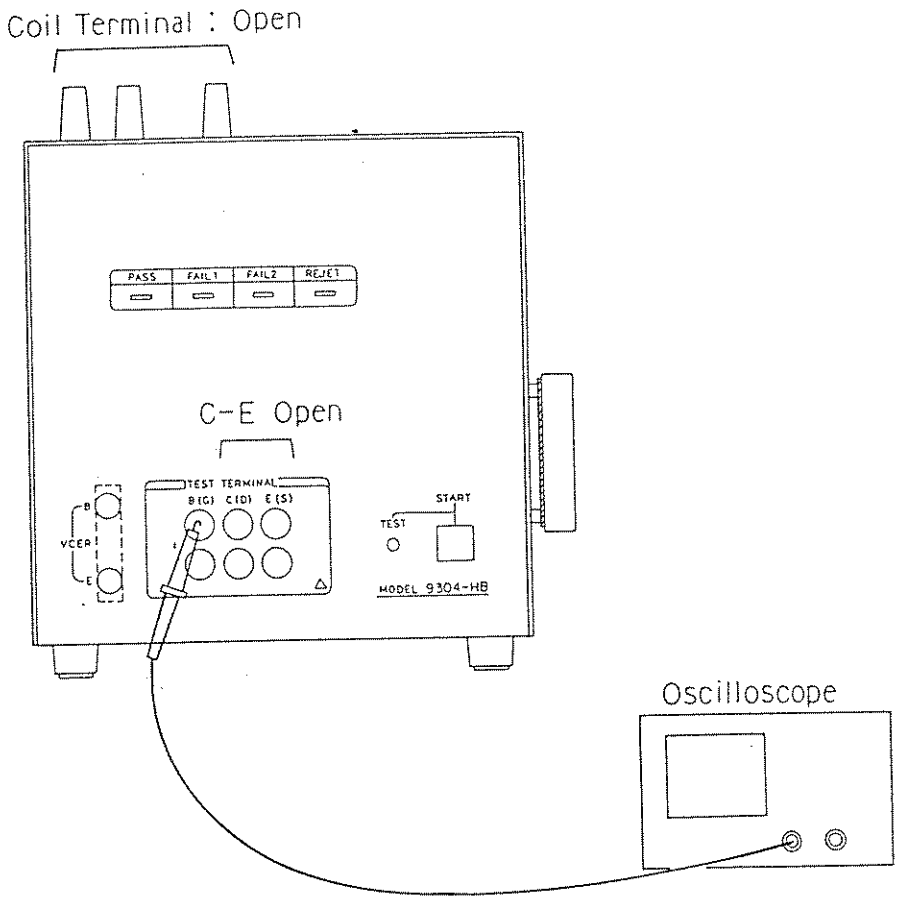


Figure 6.3a

6.3.1 V_G Calibration Procedure

Carry out the following steps to check the V_G calibration.

(a) Set the polarity to N-FET or P-FET.

(b) Open the coil terminals and the C-E line.

(c) Set V_G to any desired value.

(d) Get a reading of voltage waveform at the B(G) terminal with an oscilloscope.

(e) Trigger the oscilloscope at the fall edge of the check terminal $\overline{\text{IC ON}}$ on the 9302-LV rear panel.

Item	Measurement Range	Accuracy	Resolution
VG VGR	1.0 ~ 30.0 V	±(2% + 0.6 V)	0.1 V

6.3.2 When No V_G is Applied

Check the VG GEN board (PT9322) in the 9304-HB on the following points.

(a) VG (+ side)

Connect an oscilloscope (or DVM) to the check terminal TP4 and confirm that the exact value of voltage as programmed is applied.

(b) VGR (- side)

Connect an oscilloscope (or DVM) to the check terminal TP6 and confirm that the exact value of voltage as programmed is applied.

(c) If the voltage is clamped about 3 V, check whether or not the relay K4 on the B-E CLAMP board (PT9324) is shorted.

6.3.3 When Exact Value of V_G As Preset is Not Applied

Check the VG GEN Board (PT9322) on the following points.

(a) D/A Converter circuit adjustment of VG (+ side)

Confirm that the D/A converter DAC811JP (IC4) outputs the exact value of voltage as programmed.

(i) Connect a DVM between the check terminals TP1 and TP0.

(ii) Set the polarity to N-FET and V_G to 0 V. Push the start switch.
Adjust the variable resistor VR2 to make the offset value of the OP1 op-amp be ±0.1 mV or less.

(iii) Connect a DVM between the check terminals TP5 and TP0.
Adjust the variable resistor VR3 to make the offset value of the OP2 op-amp be ±0.1 mV or less.

(iv) Set the polarity to N-FET and V_G to 30 V. Push the start switch.
Adjust the variable resistor VR1 to have the DVM read +3.000 V (±0.001 V).

(v) Repeat the steps (ii) to (iv) above until the desired readings are obtained.

(vi) Confirm that the exact value of V_G as programmed is applied with the V_G range of 0 V to 30 V.

VG/VGR (V)	Output (V)
0.0	0.00 m
0.1	±10.00 m
0.2	±20.00 m
0.4	±40.00 m
0.8	±80.00 m
1.6	±160.0 m
3.2	±320.0 m
6.4	±640.0 m
12.8	±1.280
25.6	±2.560
30.0	±3.000

(b) D/A Converter circuit adjustment of V_G (- side)

Confirm that the D/A converter DAC811JP (IC5) outputs the exact value of voltage as programmed as follows.

(i) Connect a DVM between the check terminals TP7 and TP0.

(ii) Set the polarity to P-FET and V_G to 0 V. Push the start switch.
Adjust the variable resistor VR5 to make the offset value of the OP3 op-amp be ±0.1 mV or less.

(iii) Set the polarity to P-FET and V_G to 30 V. Push the start switch.
Adjust the variable resistor VR4 to have the DVM read -3.000 V (±0.001 V).

(iv) Repeat the steps (ii) and (iii) above until the desired readings are obtained.

(v) Confirm that the exact value of V_G as programmed is applied with the range of 0 V to 30 V.

(c) Voltage booster circuit adjustment of V_G (+ side)

(i) Connect a DVM between the check terminals TP4 and TP0.

(ii) Set the polarity to N-FET and V_G to 0 V. Push the start switch.
Adjust the variable resistor VR6 to have the DVM read ±0.1 mV or less.

(iii) Confirm the exact value of V_G as programmed is applied with the range of 1 V to 30 V.

(d) Voltage booster circuit adjustment of V_G (- side)

(i) Connect a DVM between the check terminals TP6 and TP0.

(ii) Set the polarity to P-FET and V_G to 0 V. Push the start switch. Adjust the variable resistor VR7 to have the DVM read ±0.1 mV or less.

(iii) Confirm the exact value of V_G as programmed is applied with the range of 1 V to 30 V.

(e) Confirm that the applied voltage is polarity-reversed. Short the coil terminals and the C-E line.

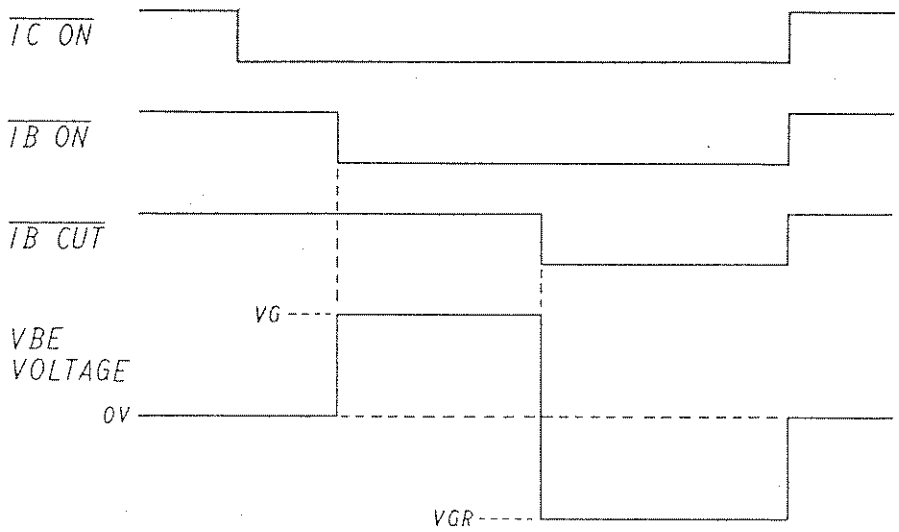
(i) Set test conditions as follows:

N-FET/P-FET

IC = 0 V	VC = –	V-GATE = 0 V
VG = 1~30 V	V-CLAMP = –	IH = 0 A
VGR = 1~30 A		IL = 0 A

(ii) Connect an oscilloscope to the check terminal $\overline{\text{IB CUT}}$ on the 9302-LV rear panel. Push the start switch and confirm that $\overline{\text{IB CUT}}$ signals are output.

(iii) Connect an oscilloscope to the B(G) terminal and push the start switch. Confirm that the voltage waveform at the B(G) terminal is as shown below.



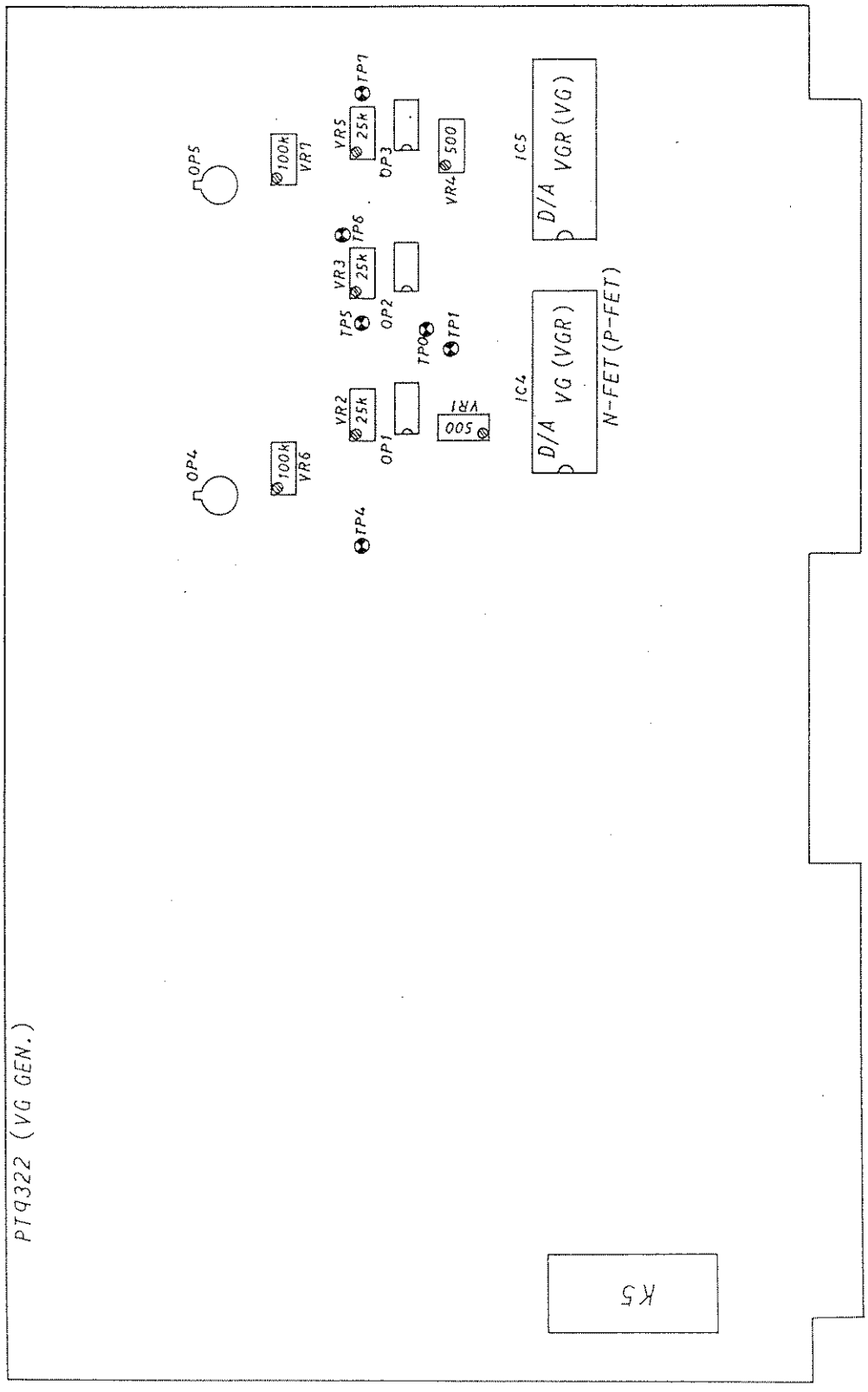


Figure 6.3b VG GEN Board (PT9322)

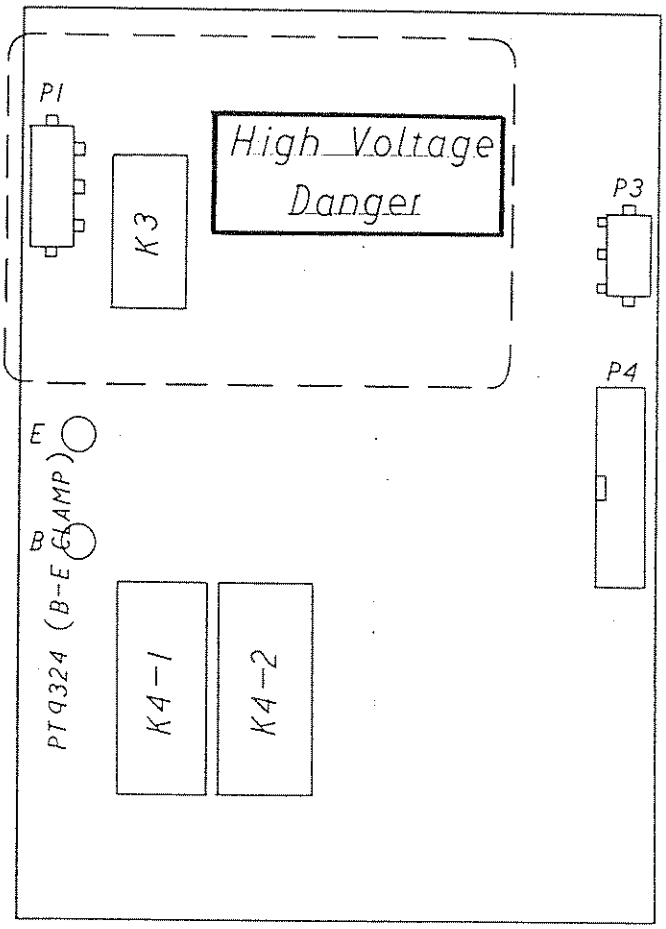


Figure 6.3c B-E CLAMP Board (PT9324)

6.4 V-CLAMP Adjustment

The adjustment of high voltage power source is accompanied by great danger. Be sure to turn off the power supply and wait 5 minutes before starting the adjustment of the inside of the 9302-LV or the 9304-HB.

6.4.1 V-CLAMP Adjustment Procedure

(a) Connect a voltage probe (1000 : 1) to the DVM.

(b) Connecting points of the DVM are as follows:

- Inside of 9304-HB: between the plus side of the condenser C1 and the minus side of the condenser C6
- Inside of 9302-LV: between the check terminals TP4 and TP0 on the HV CONTROL board (PT9328)

(c) V-CLAMP is set without pushing the start switch.

(d) Set V-CLAMP at any desired value.

(e) Get a reading of applied voltage.

Item	Measurement Range	Accuracy	Resolution
V-CLAMP	VC = OFF 40~2000 V	±1%	1 V
	VC = ON 30~2000 V		

6.4.2 When No V-CLAMP is Applied

(a) If the value of V-CLAMP is more than ±1% of the preset value, the light of the V-CLAMP READY lamp on the 9302-LV front panel goes off.

(b) When V-CLAMP is set to 0 V, it takes the machine a long time to complete discharge, resulting in lights-out of the V-CLAMP READY lamp for a long time.

6.4.3 When Exact Value of V-CLAMP As Preset is Not Applied

(a) HV CONTROL board (PT9328) in 9302-LV

(i) Pull out the following:
#5 (PT9327-001), #6 (PT9327-000), #7 (PT9327-000)

(ii) Open the coil terminals.

(iii) Pull out the +HV and -HV cables.

(iv) Short the check terminals TP3 and TP4 with a clip.

(v) Connect a DVM between the check terminals TP4 and TP0.

(vi) Confirm that the exact value of V-CLAMP as programmed is applied with the range of 40 V to 200 V.

(b) D/A converter circuit of HV CONTROL board

(i) Pull out the following:
#5 (PT9327-001), #6 (PT9327-000), #7 (PT9327-000)

(ii) Connect a DVM between the check terminals TP1 and TP0.

(iii) Set V-CLAMP to 0 V and adjust the variable resistor VR5 to have the DVM read 0.00 mV (± 0.10 mV).

(iv) Set V-CLAMP to 2000 V and adjust the variable resistor VR4 to have the DVM read -10.000 V (± 0.001 V).

(v) Repeat the steps (iii) and (iv) above until the desired readings are obtained.

(vi) Confirm that the exact value of V-CLAMP as programmed is applied with the range of 0 V to 2000 V.

V-CLAMP (V)	Output (V)
0	0.00 m
1	-5.00 m
2	-10.00 m
4	-20.00 m
8	-40.00 m
16	-80.00 m
32	-160.0 m
64	-320.0 m
128	-640.0 m
256	-1.280
512	-2.560
1024	-5.120
2000	-10.000

(vii) Set V-CLAMP to 0 V and short the check terminals TP3 and TP4 with a clip.

(viii) Connect a DVM between the check terminals TP4 and TP0.

(ix) Set V-CLAMP to 1 V and adjust the variable resistor VR3 to have the DVM read 1000.0 mV (±0.5 mV).

(c) HV GEN board #7 (PT9327-000)

(i) Pull out the following:

#5 (PT9327-001), #6 (PT9327-000), #8 (PT9328)

(ii) Open the coil terminals.

(iii) Pull out the +HV and -HV cables.

(iv) Adjust the 200 V circuit as follows:

(1) Set V-CLAMP to 0 V and have the applied voltage be 0 V.

(2) Connect a DVM between the check terminals TP2 and TP1.

(3) Set V-CLAMP to 300 V and adjust the variable resistor VR1 to have the applied voltage be 199.0 V (±1.0 V).

(v) Adjust the 400 V circuit as follows:

(1) Set V-CLAMP to 0 V and have the applied voltage be 0 V.

(2) Connect a DVM between the check terminals TP4 and TP3.

(3) Set V-CLAMP to 500 V and adjust the variable resistor VR2 to have the applied voltage be 199.0 V (±1.0 V).

(vi) Adjust the 600 V circuit as follows:

(1) Set V-CLAMP to 0 V and have the applied voltage be 0 V.

(2) Connect a DVM between the check terminals TP6 and TP5.

(3) Set V-CLAMP to 700 V and adjust the variable resistor VR3 to have the applied voltage be 199.0 V (±1.0 V).

(vii) Adjust the 800 V circuit as follows:

(1) Set V-CLAMP to 0 V and have the applied voltage be 0 V.

(2) Connect a DVM between the check terminals TP8 and TP7.

(3) Set V-CLAMP to 900 V and adjust the variable resistor VR4 to have the applied voltage be 199.0 V (±1.0 V).

(d) HV GEN board #6 (PT9327-000)

(i) Pull out the following:

#5 (PT9327-001), #6 (PT9327-000), #8 (PT9328)

(ii) Carry out the steps of (c) above by referring to Figure 6.4a HV-MATRIX.

(e) HV GEN board #5 (PT9327-001)

(i) Pull out the following:

#6 (PT9327-000), #7 (PT9327-000), #8 (PT9328)

(ii) Carry out the steps of (c) above by referring to Figure 6.4a HV-MATRIX.

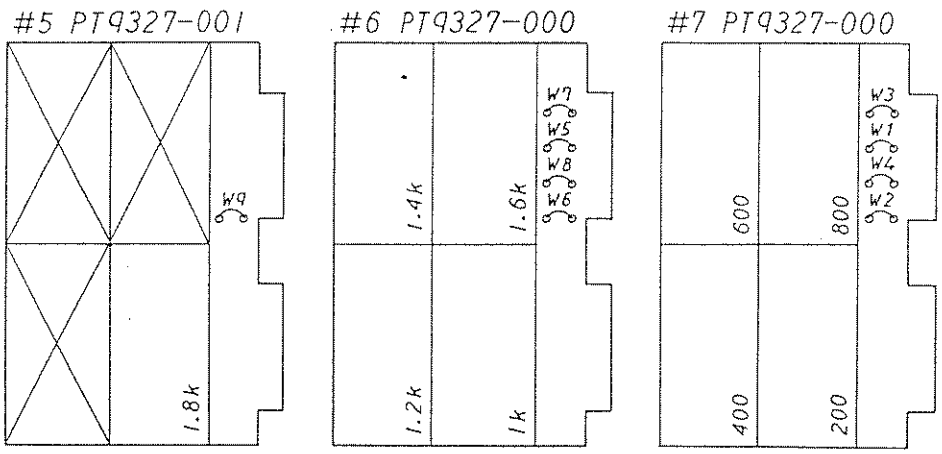
(f) Re-adjustment of Gain

(i) Connect a voltage probe (1000 : 1) to the DVM.

(ii) Connect a DVM between the check terminals TP4 and TP0 on the HV CONTROL board (PT9328).

(iii) Set V-CLAMP to 1000 V and adjust the variable resistor VR4 to have the DVM read 1000.0 mV (±1.0 mV).

(vi) Confirm that the exact value of V-CLAMP as programmed is applied with the range of 0 V to 2000 V.



V-CLAMP	1.8K W9	1.6K W8	1.4K W7	1.2K W6	1K W5	800 W4	600 W3	400 W2	200 W1
1801V — 2000V	○	○	○	○	○	○	○	○	○
1601 — 1800	/	○	○	○	○	○	○	○	○
1401 — 1600	/	/	○	○	○	○	○	○	○
1201 — 1400	/	/	/	○	○	○	○	○	○
1001 — 1200	/	/	/	/	○	○	○	○	○
801 — 1000	/	/	/	/	/	○	○	○	○
601 — 800	/	/	/	/	/	/	○	○	○
401 — 600	/	/	/	/	/	/	/	○	○
201 — 400	/	/	/	/	/	/	/	/	○
0 — 200	/	/	/	/	/	/	/	/	/

HV — MATRIX

Figure 6.4a HV-MATRIX

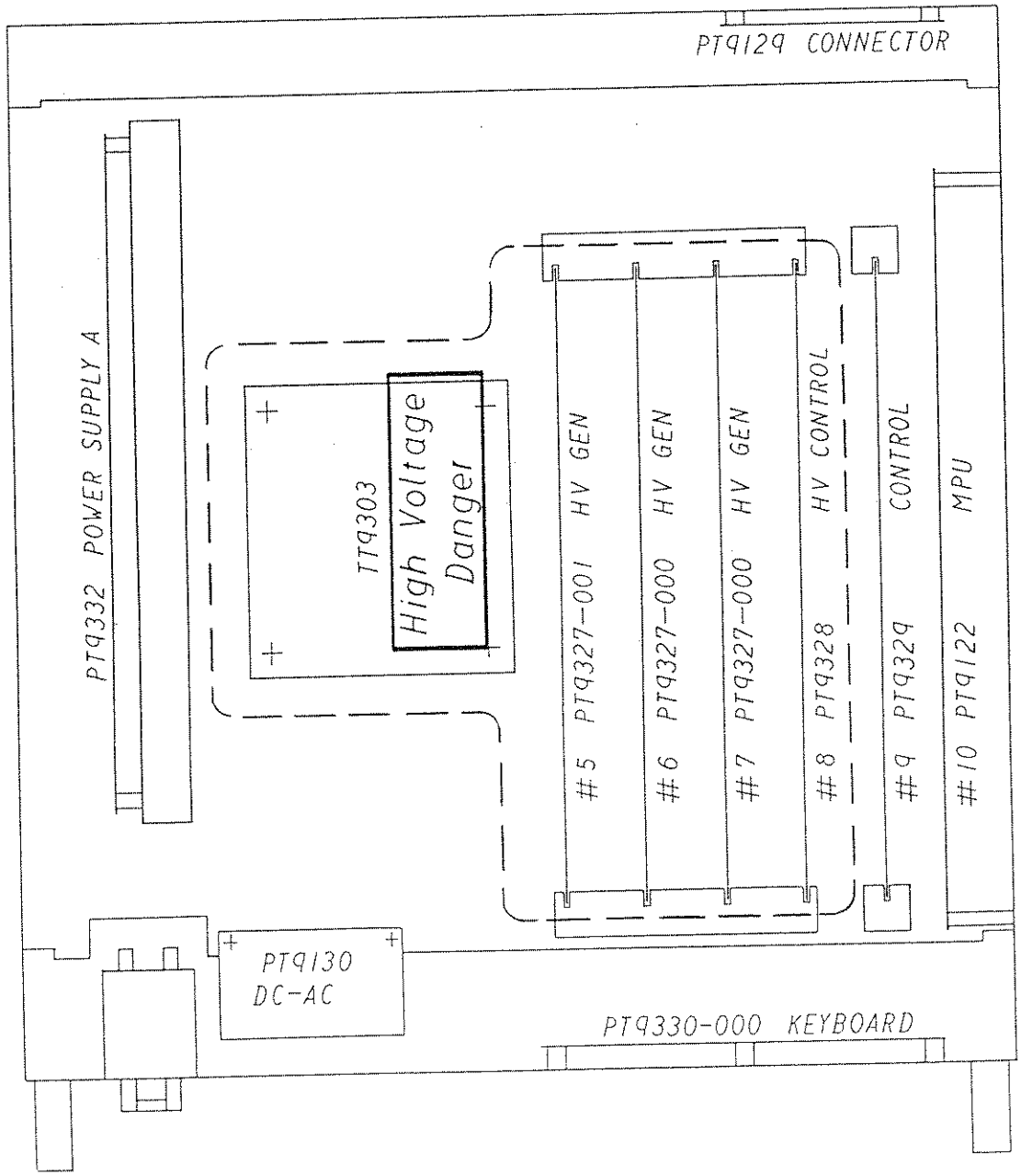


Figure 6.4b 9302-LV Top View

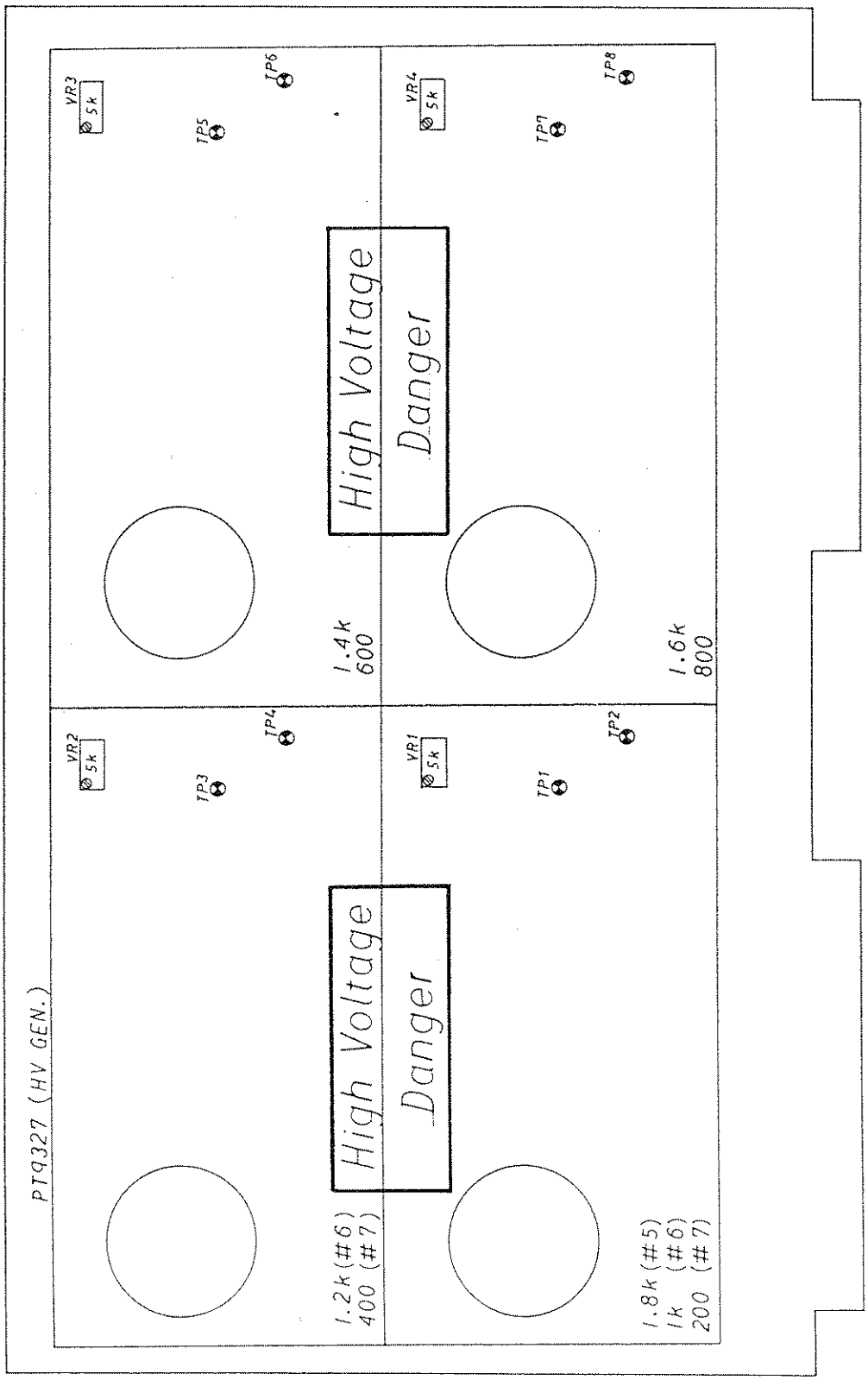


Figure 6.4c HV GEN Board (PT9327)

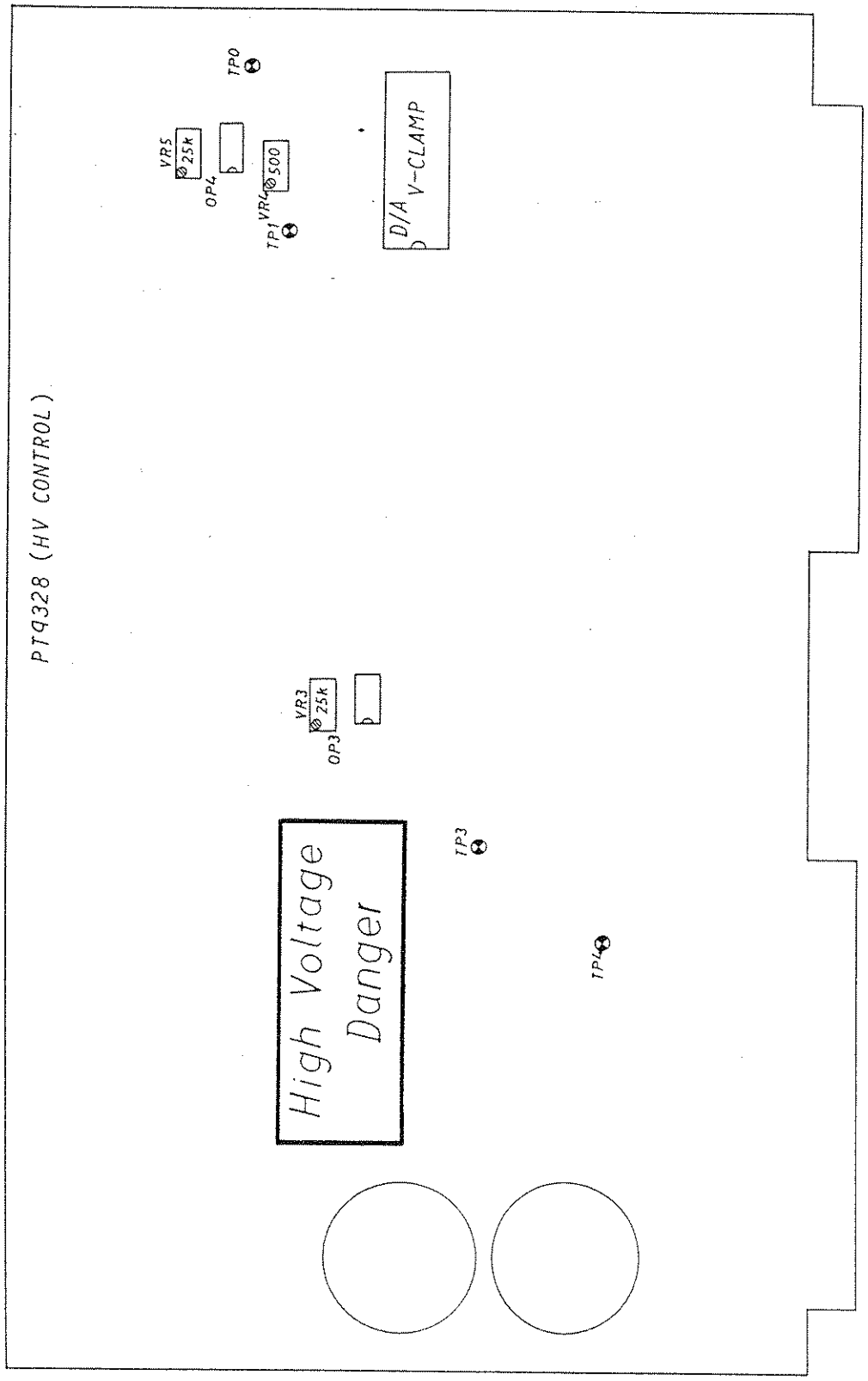


Figure 6.4d HV CONTROL (PT9328)

6.5 DETECTOR Circuit Adjustment

Adjust the DETECTOR board (PT9323) in the 9304-HB by the following steps.
Before starting the adjustment, open the coil terminals and the C-E line.

6.5.1 D/A Converter Adjustment

(1) V-GATE adjustment

(a) Connect a DVM between the check terminals TP8 and TP0.

(b) Set the polarity to N-TR. and V-GATE to 0 V. Push the start switch and adjust the variable resistor VR5 to have the DVM read 0.00 mV (±0.1 mV).

(c) Set the polarity to N-TR. and V-GATE to 2000 V. Push the start switch and adjust the variable resistor VR4 to have the DVM read +5.000 V (±0.001 V).

(d) Set the polarity to P-TR. and V-GATE to 2000 V. Push the start switch and confirm that the DVM reads -5.000 V (±0.001 V).

(e) Repeat the steps (b) to (d) above until the desired readings are obtained.

(f) Confirm that the exact value of V-GATE is applied with the range of 0 V to 2000 V.

V-GATE (V)	Output (V)
0	0.00 m
1	±2.50 m
2	±5.00 m
4	±10.00 m
8	±20.00 m
16	±40.00 m
32	±80.00 m
64	±160.0 m
128	±320.0 m
256	±640.0 m
512	±1.280
1024	±2.560
2000	±5.000

(2) I_C Calibration

(a) Connect a DVM between the check terminals TP11 and TP0.

(b) Set the polarity to N-TR. and I_C to 0 A. Push the start switch and adjust the variable resistor VR8 to have the DVM read 0.00 mV (±0.1 mV).

(c) Set the polarity to N-TR. and I_C to 100 A. Push the start switch and adjust the variable resistor VR7 to have the DVM read -5.000 V (±0.001 V).

(d) Set the polarity to P-TR. and I_C to 100 A. Push the start switch and confirm that the DVM reads +5.000 V (±0.001 V).

(e) Repeat the steps (b) to (d) above until the desired readings are obtained.

(f) Confirm that the exact value of I_C is applied with the range of 0 A to 100 A.

IC/IH/IL (A)	Output (V)
0.0	0.00 m
0.1	∓5.00 m
0.2	∓10.00 m
0.4	∓20.00 m
0.8	∓40.00 m
1.6	∓80.00 m
3.2	∓160.0 m
6.4	∓320.0 m
12.8	∓640.0 m
25.6	∓1.280
51.2	∓2.560
100.0	∓5.000

(3) I_H Calibration

Carry out the steps of (2) above by referring to the circuit schematics.

(4) I_L Calibration

Carry out the steps of (2) above by referring to the circuit schematics.

6.5.2 Offset Adjustment

(1) Op-amp (5B)

(a) Connect a DVM between the check terminals TP5 and TP0.

(b) Adjust the variable resistor VR1 to have the DVM read 0.00 mV (±0.2 mV).

(2) Op-amp (6B)

(a) Connect a DVM between the check terminals TP6 and TP0.

(b) Adjust the variable resistor VR2 to have the DVM read 0.00 mV (±0.2 mV).

6.5.3 A/D Converter Adjustment

- Cut the jumper JC or detach the VCL-ERR circuit (or detach R49 and R51).
- Disconnect the connector P1 (VC) on the board and connect P2 (IC).
- Detach the software check routine by referring to Figure 6.5a. The MPU board (PT9122) is installed in the 9302-LV. The initial setting of the CPU is executed by turning off the power supply once and turn it on.

(1) Gain offset adjustment when the S/H amplifier is in a sample state

Open the coil terminals and the C-E line.

(a) Set the test conditions as follows. (The underlined items are important.)

N-TR	IC = 5 A	VC = –	V-GATE = 0 V
	IB = 0 A	V-CLAMP = –	IH = 0 A
	IBR = –		IL = 0 A

(b) Disconnect every check terminal on the board.

(c) Push the start switch. Adjust the variable resistor VR17 to have 0 V (±0 V) displayed on the LCD screen.

(d) Connect the standard power source to the check terminal TP3 and apply +5.000 V. Disconnect the other check terminals.

(e) Push the start switch and adjust the variable resistor VR16 to have +2000 V (±1 V) displayed on the LCD screen.

(f) Apply -5.000 V to the check terminal TP3.

(g) Push the start switch and confirm that -2000 V (±1 V) is displayed on the LCD screen.

(h) Repeat the steps (b) to (g) above until the desired states are obtained.

(i) Confirm the linearity by referring to the following table.

Input (V)	Display (V)
0.00 m	0
±2.50 m	±1
±5.00 m	±2
±10.00 m	±4
±20.00 m	±8
±40.00 m	±16
±80.00 m	±32
±160.0 m	±64
±320.0 m	±128
±640.0 m	±256
±1.280	±512
±2.560	±1024
±5.000	±2000

(2) Offset error calibration when the S/H amplifier is in a hold state

Open the coil terminals and the C-E line.

(i) Set the test conditions as follows. (The underlined items are important.)

N-TR	IC = 0 A	VC = –	V-GATE = 0 V
	IB = 0 A	V-CLAMP = –	IH = 0 A
	IBR = –		IL = 0 A

(ii) Push the start switch. Connect an oscilloscope to the TP22 or the jumper JB and confirm that S/H signals are output.

(iii) Disconnect every check terminal on the board.

(vi) Push the start switch and confirm that 5 to 7 V is displayed on the LCD screen.

(v) Push the start switch. Adjust the variable resistor VR17 to have 0 V (±0 V) displayed on the LCD screen.

Note: Make a jumper for the jumper JC.

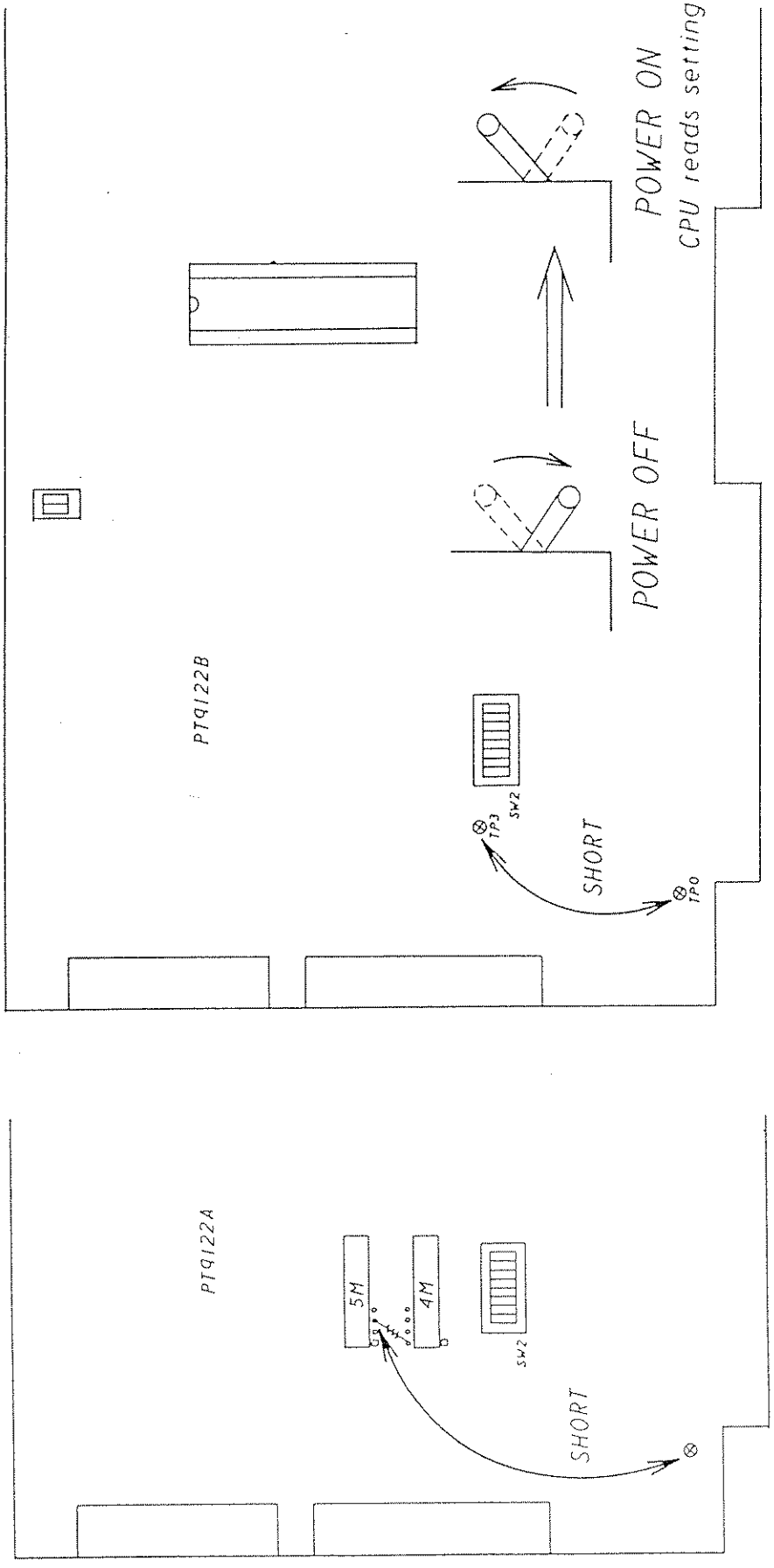


Figure 6.5a How to Detach Software Check Routine

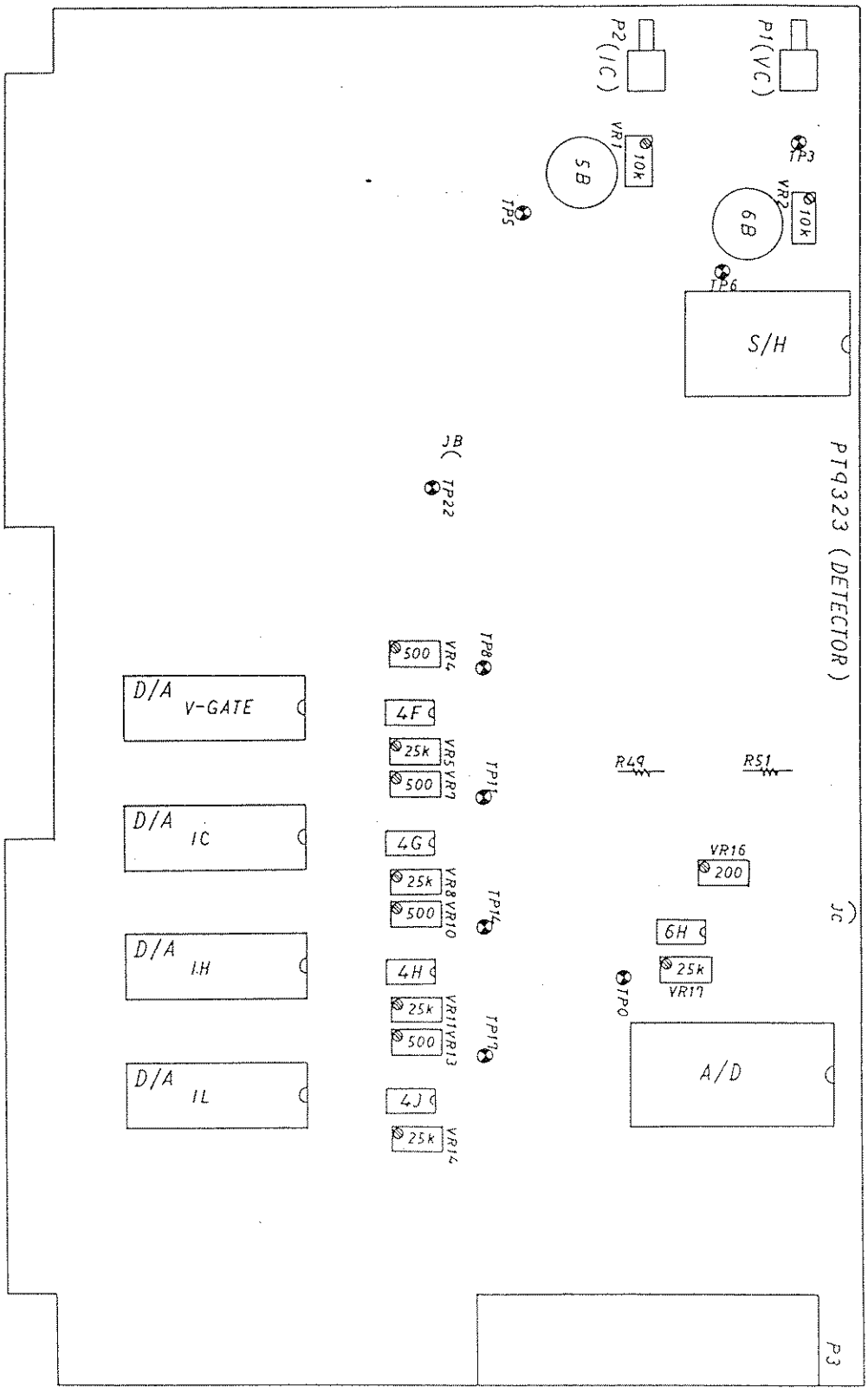


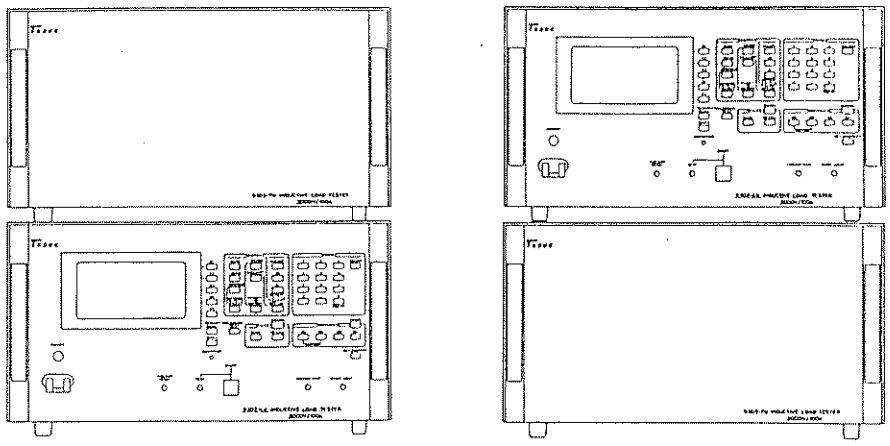
Figure 6.5b DETECTOR Board (PT9323)

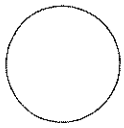
APPENDIX

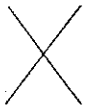
A. CAUTION FOR HANDLING

(1) Place surely the 9303-PU on the 9302-LV.

(2) Never put any heavy equipment on the 9302-LV and 9303-PU.







(3) High voltage power source, very dangerous, is located in the 9302-LV and 9304-HB. Wait for 5 minutes before starting maintenance work by removing a cover.

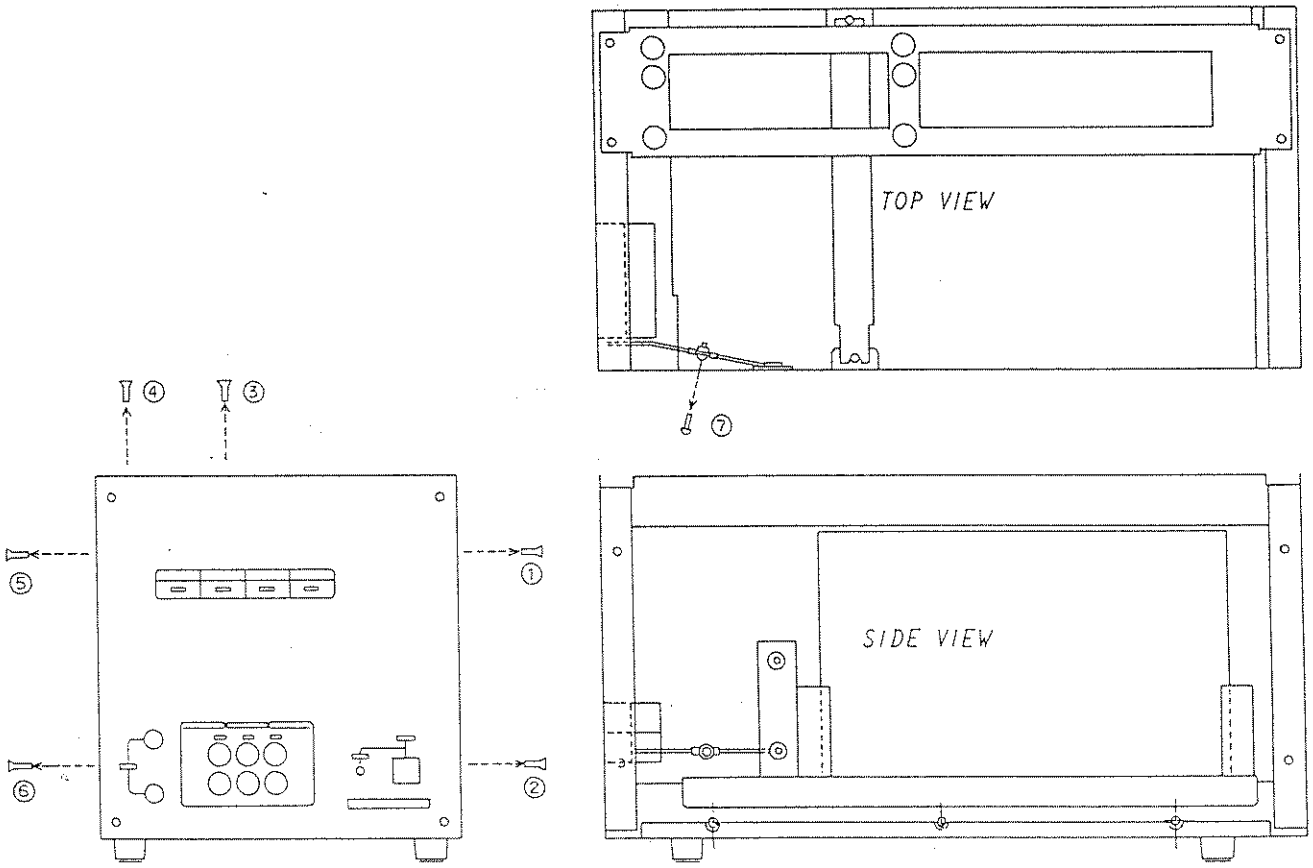
B. PARAMETRIC VALUES OF COILS

Nominal value (μH)	Measured value (μH)	Q	Resistance (mΩ)
50	50.0	1.605	38
100			
200	203	4.95	55
300	297	6.94	70
500	504	6.33	100

Remark : at measurement of 1 kHz

C. PEPRACEMENT OF FRONT PANEL

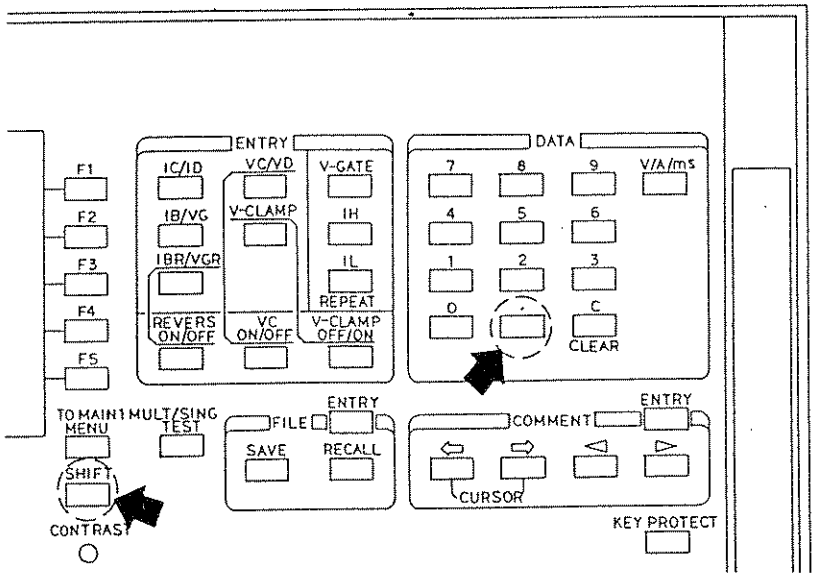
After removing the cover, detach the screws-①to⑦indicated in the figure below. Then, detach the front panel together with the frame.



FRONT PANEL

D. POWER OFF IN LONG TERM

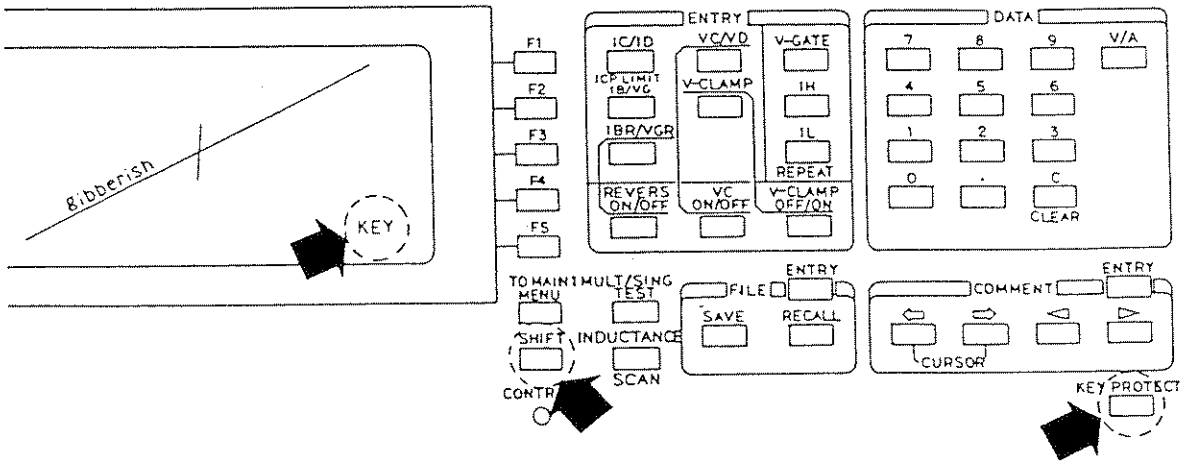
□ If the inductive load tester is powered off for about one month, the installed battery may be dead, which results in an improper display of the LCD screen. In that case, press the SHIFT-key and the •-key at a time to execute the initial reset. The program settings get those which are made at the shipment of the inductive load tester.



□ If the inductive load tester is unable to be initialized, the P-ROM replacement may have caused an improper display on the LCD screen and the activation of the KEY PROTECT function. When "KEY" appears on the lower right side of the screen, do the following.

(i) Press the SHIFT-key and the KEY PROTECT key at the same time to inactivate the KEY PROTECT function.

(ii) Press the SHIFT-key and the •-key at the same time to execute the initial reset. The program settings get those that are made at the shipment of the inductive load tester.



'97.2.-4